

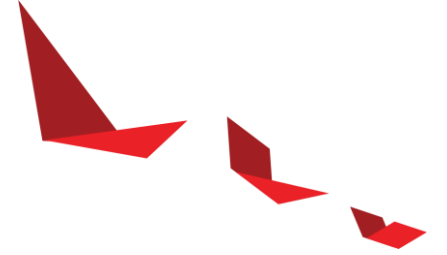


Versal™ Architecture Overview Technical Module

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March 10, 2021

Agenda

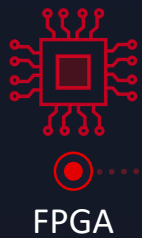
- High Level Versal Overview
- Versal Features and Capabilities
 - Overview
 - Network on Chip (NoC)
 - Processing System
 - AI Engines
 - Adaptable Engines
 - Clocking, IO, Memory Controllers
 - Gigabit Transceivers and Connectivity IP
 - Boot, Configuration, and Security
 - Power and Performance
- Product Tables and Roll Out



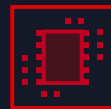
➤ Disruptive Innovation Needed: Enter ACAP

A new class of devices for
today's challenges

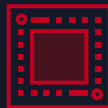
Software Programmability



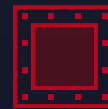
FPGA



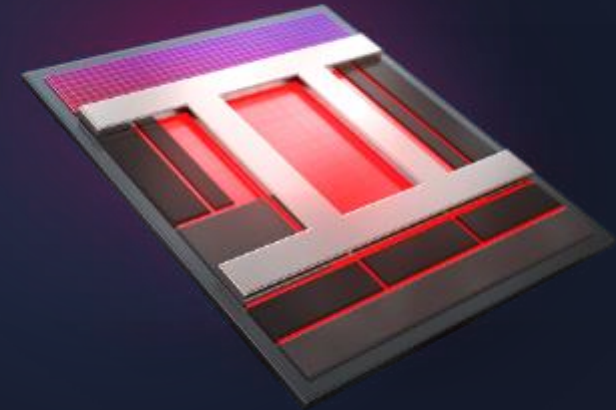
SoC



MPSoC



RFSoc

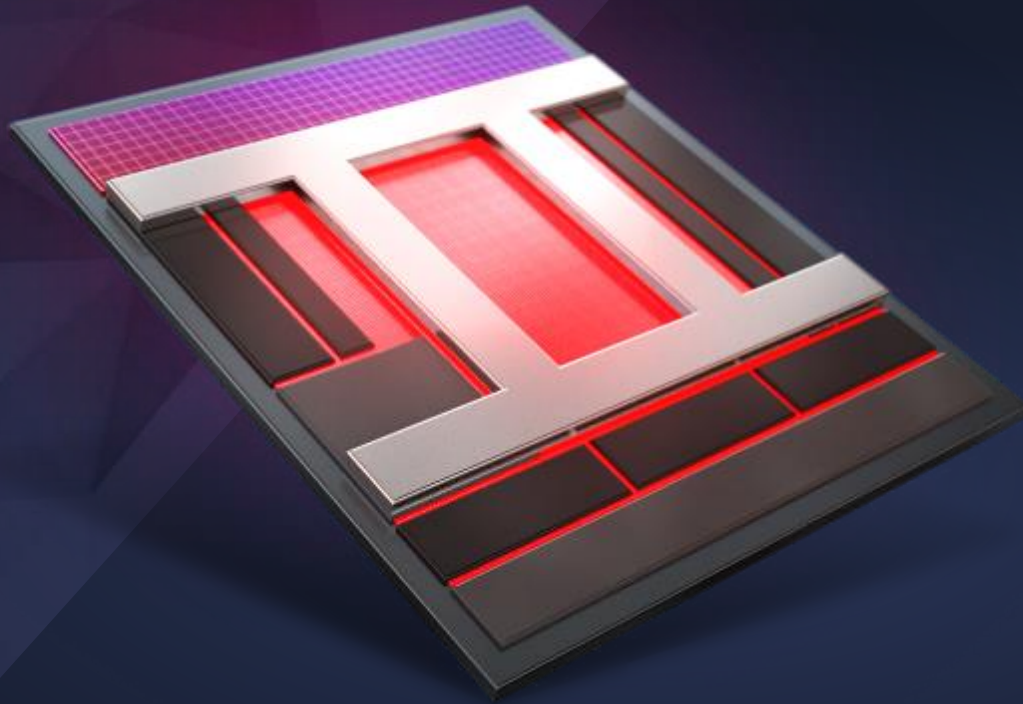


ACAP

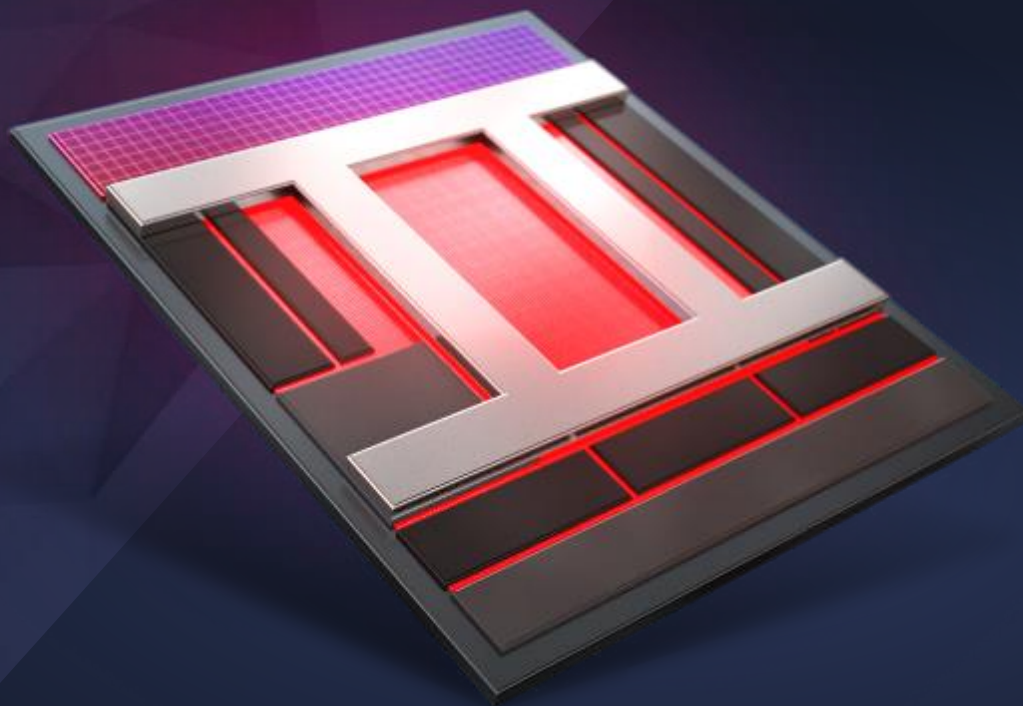
Device Category

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ACAP



Adaptive Compute Acceleration Platform

Versal Roadmap



AI Core
AI Inference
Throughout



Prime
Broadest
Application



Premium
112G Serdes
600G Cores



HBM
Memory
Integration



AI RF
AI with
Integrated RF



AI Edge
Lowest power
AI

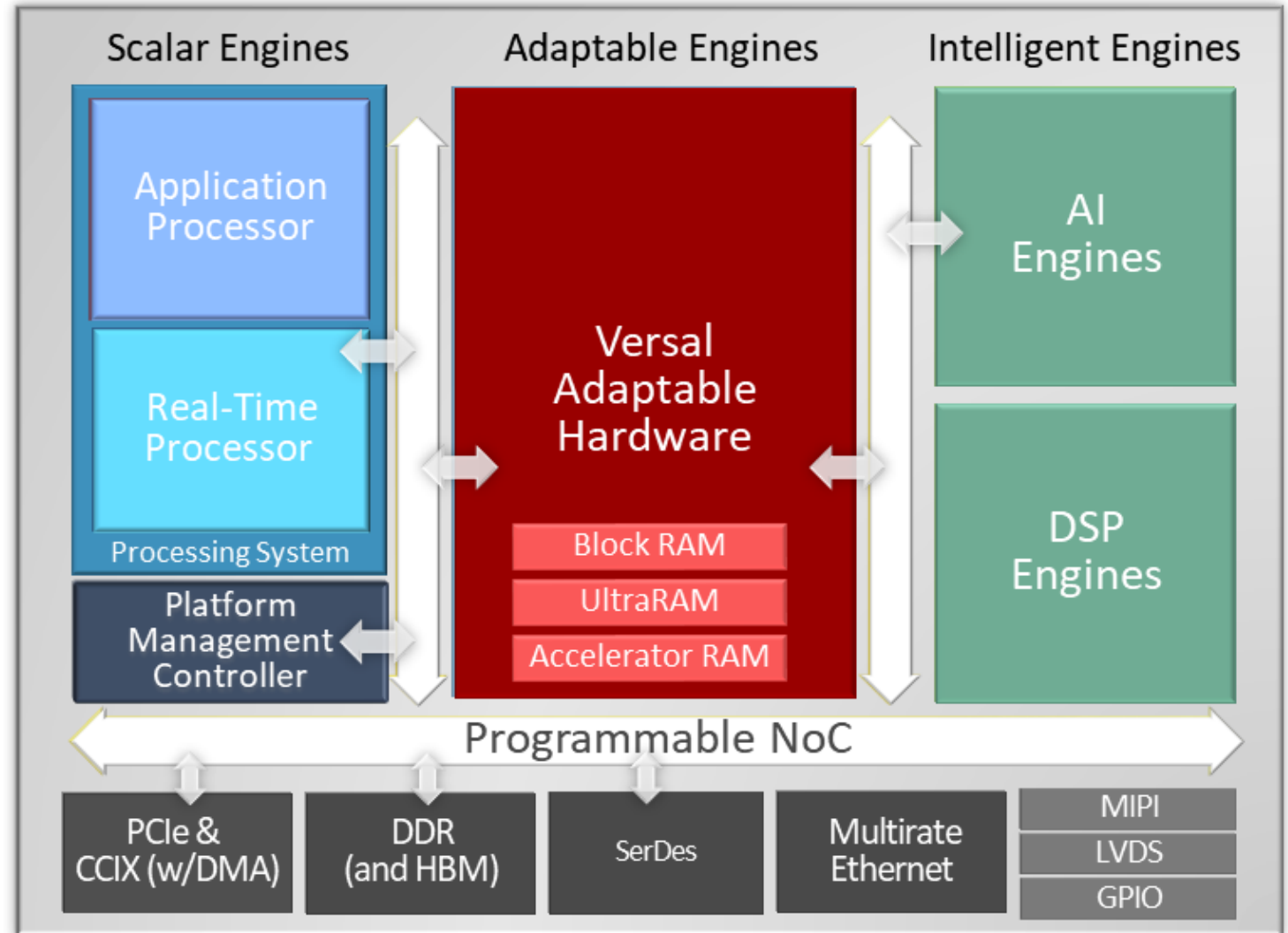
2020

2021

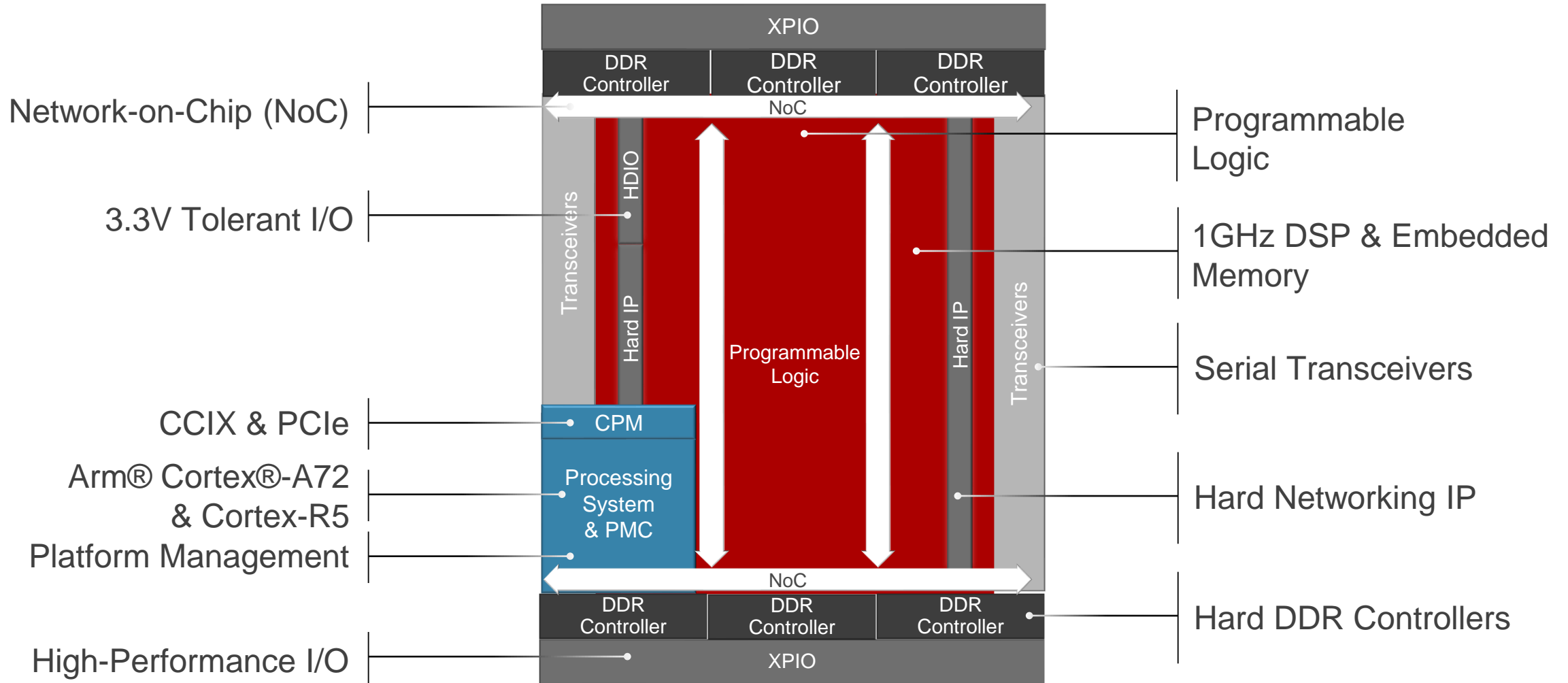
2022

Adaptable Architecture Connected Via NoC

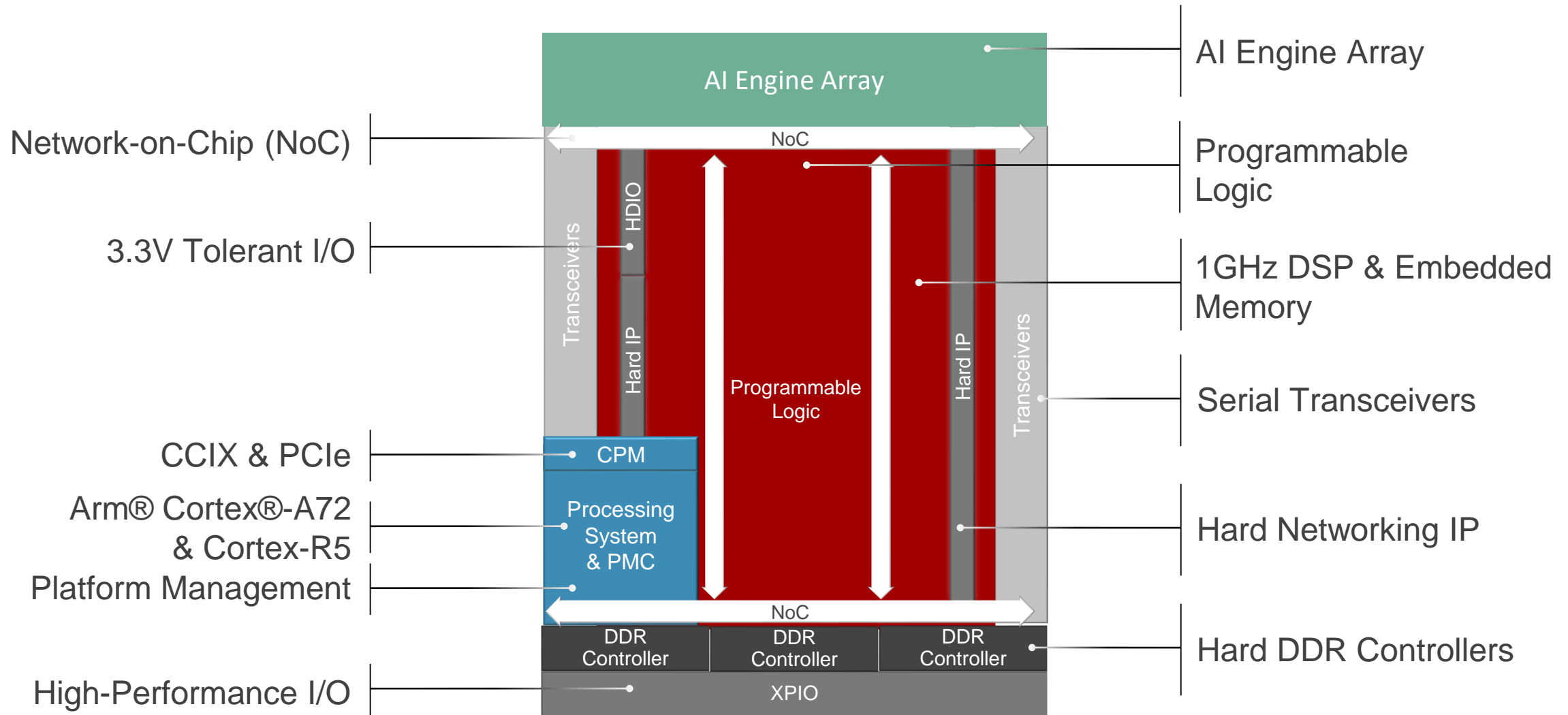
- ▶ **Scalar Engines**
 - Arm® Cortex™-A72 APU
 - Arm Cortex-R5 RPU
- ▶ **Adaptable Engines**
 - CLBs
 - Internal Memory
- ▶ **Intelligent Engines**
 - AI Engine
 - DSP Engine
- ▶ **Connectivity**
 - PCIe Gen4/5 w/CCIX
 - Ethernet, Interlaken and Cryptography
 - DDR Memory Controllers
 - Transceivers
 - I/O
- ▶ **Platform Resources**
 - Network-On-Chip
 - Platform Management Controller



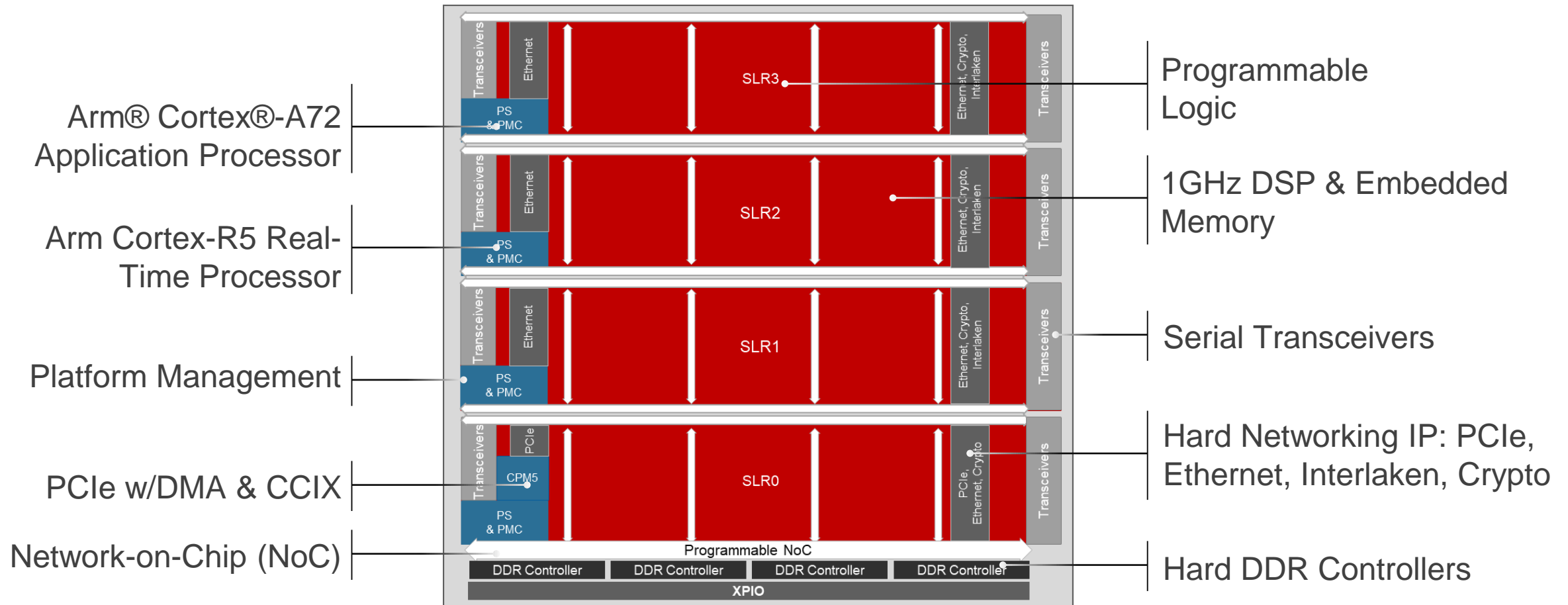
Versal™ Prime Series – Device View



Versal™ AI Core Series – Device View

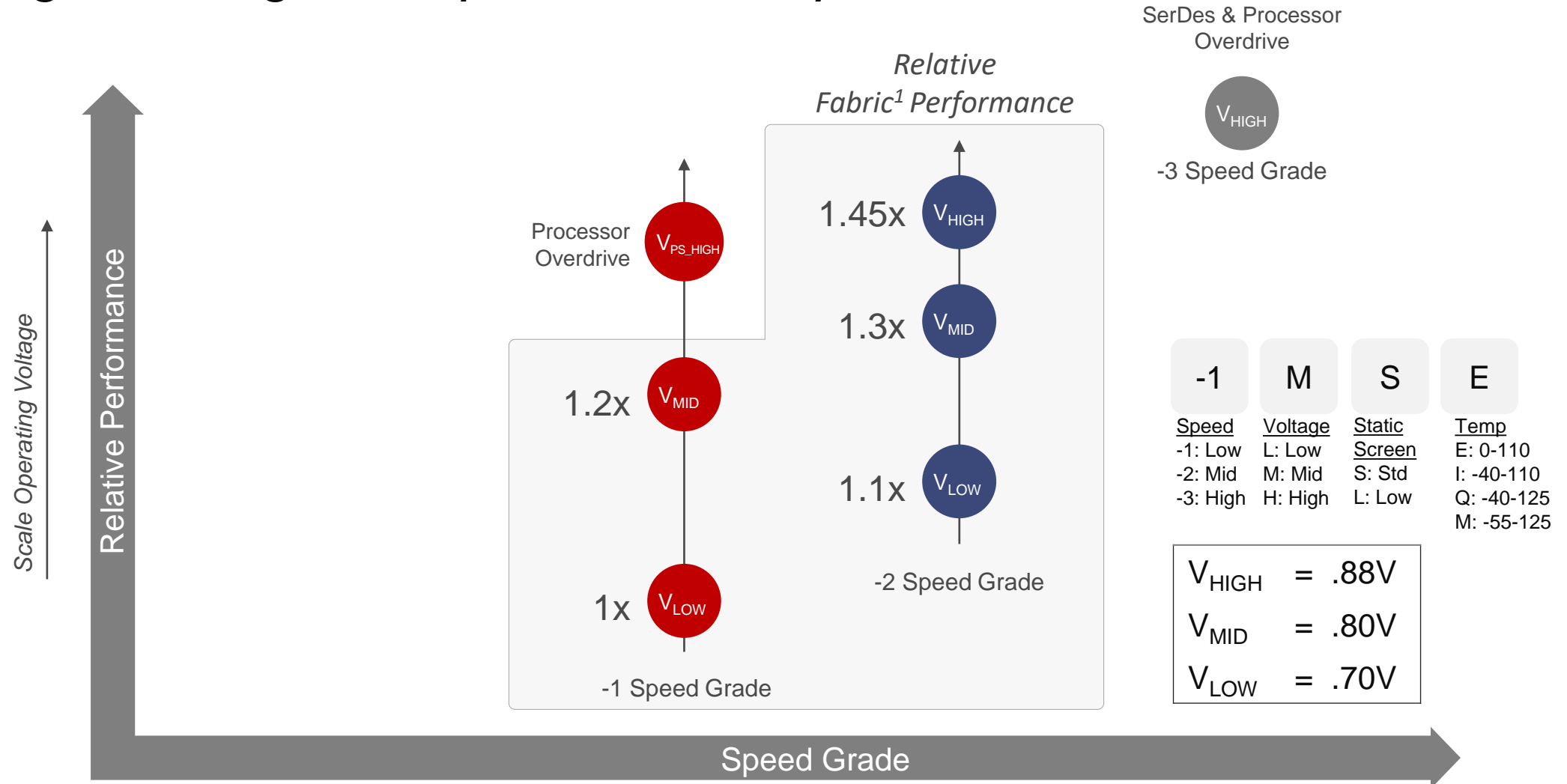


Versal™ Premium Series – Device View



Granular Control of Power vs. Performance

Voltage Scaling with Speed Grade Options

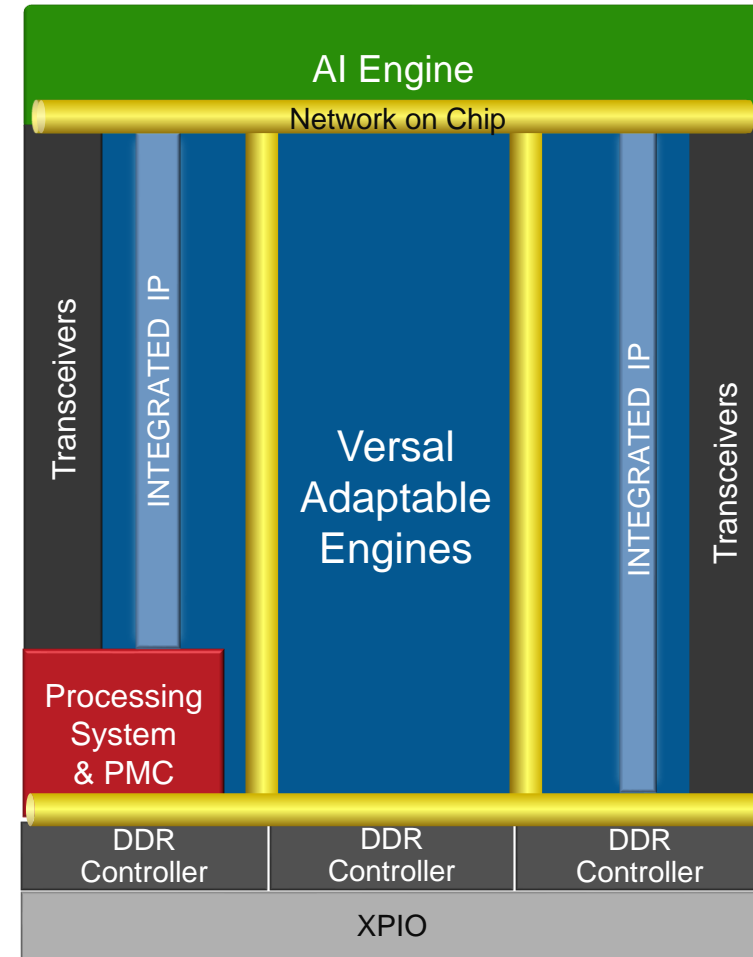


1: Programmable Logic, DSP, and Embedded RAM

Network on Chip (NoC)

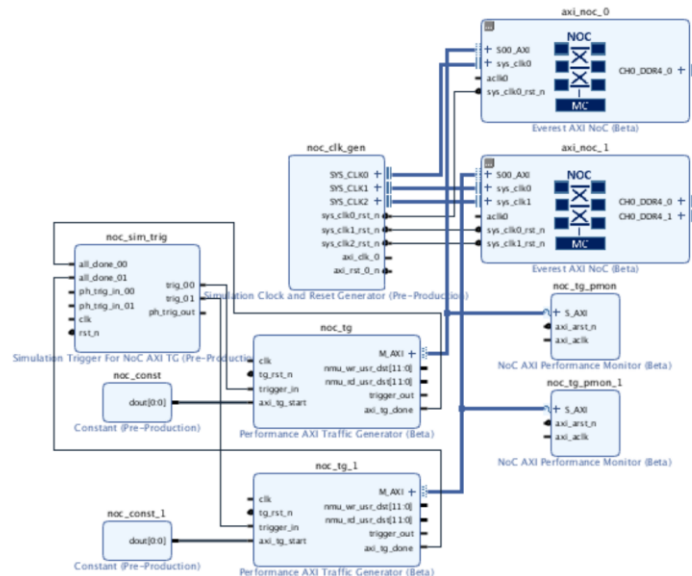
Why put the Network on Chip in Versal™ ACAPs?

- ▶ Problems that the NoC is solving
 - High Bandwidth Pipe crossing the device
 - Processor supporting multiple memory controllers
 - Interconnect pipe to
 - AI Engines
 - Processing System
 - Programmable Logic
- ▶ Problems that NoC is NOT solving
 - Does not replace traditional routing resources
 - Does not connect to
 - Soft memory controllers
 - Low latency memory interfaces: RLDRAM3, QDRIV

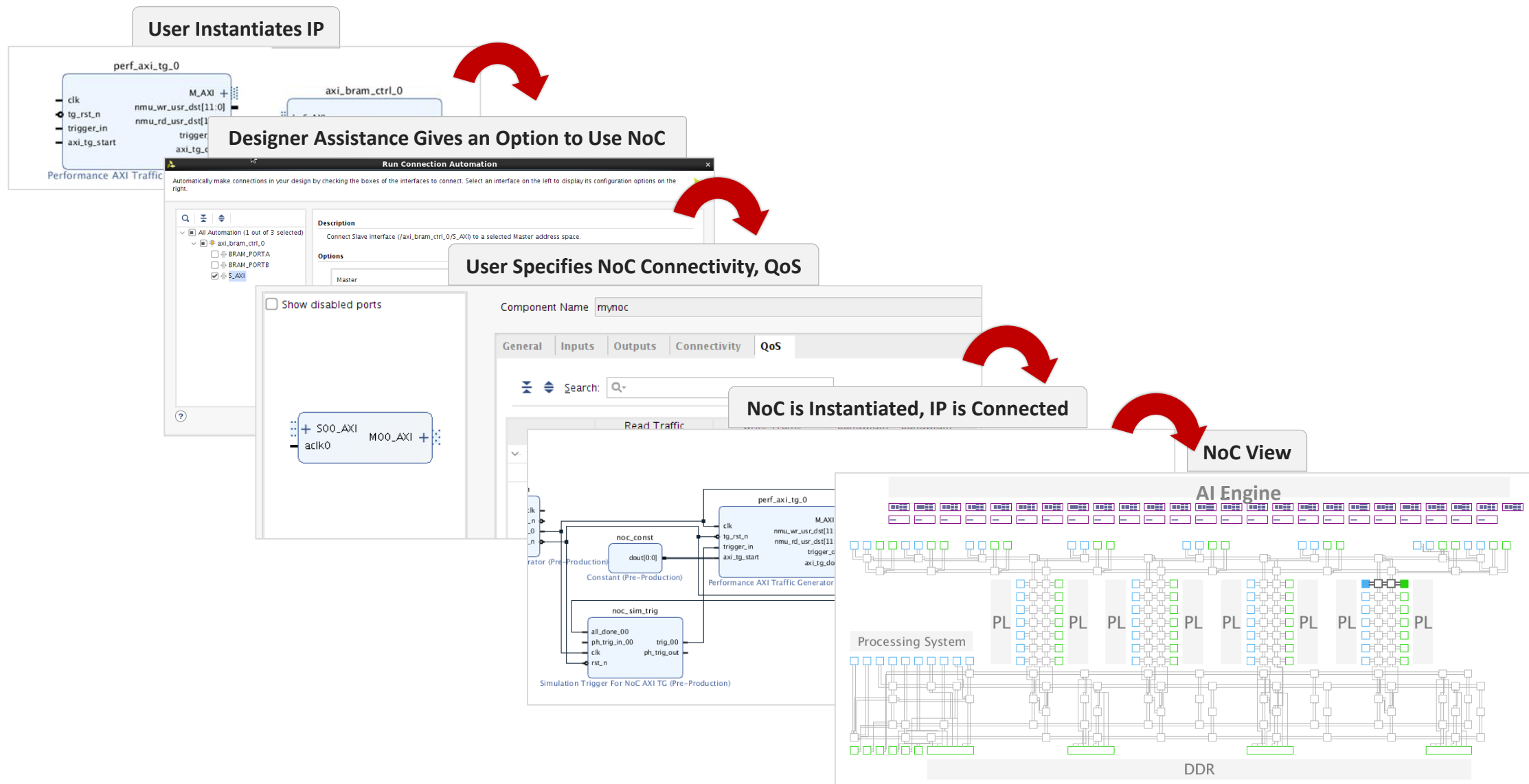


NoC Compiler

- ▶ NoC compiler takes user input QOS, Bandwidth, Latency and automatically configures NOC in a deadlock free configuration



Example IP Integrator Design Flow



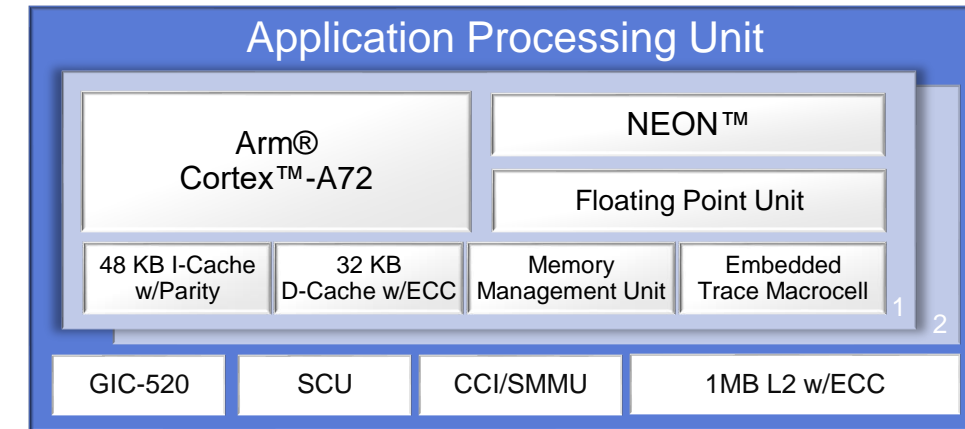


Processing System and Platform Management Controller

Scalar Engines in the Arm Processing System

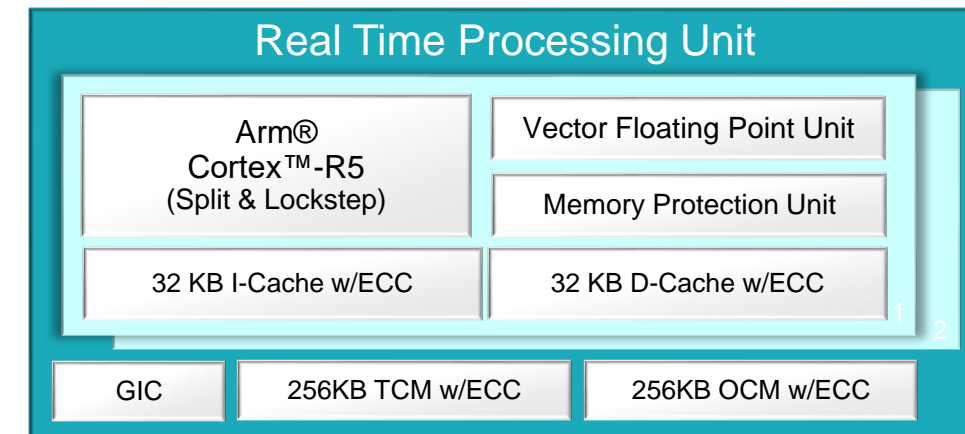
► Dual-Core Arm® Cortex™-A72 Application Processors

- Up to 1.7GHz for 2X single-threaded performance¹
- Cost and power optimized (half the power)
- Code compatibility (ARMv8-A architecture)
- Device boots without a bit stream



► Dual-Core Arm® Cortex™-R5 Real Processors

- Up to 750MHz for 1.4X greater performance¹
- Low latency and deterministic
- Flexible operation modes: Split-Mode and Lock-Step
- Highest levels of functional safety (ASIL and SIL)

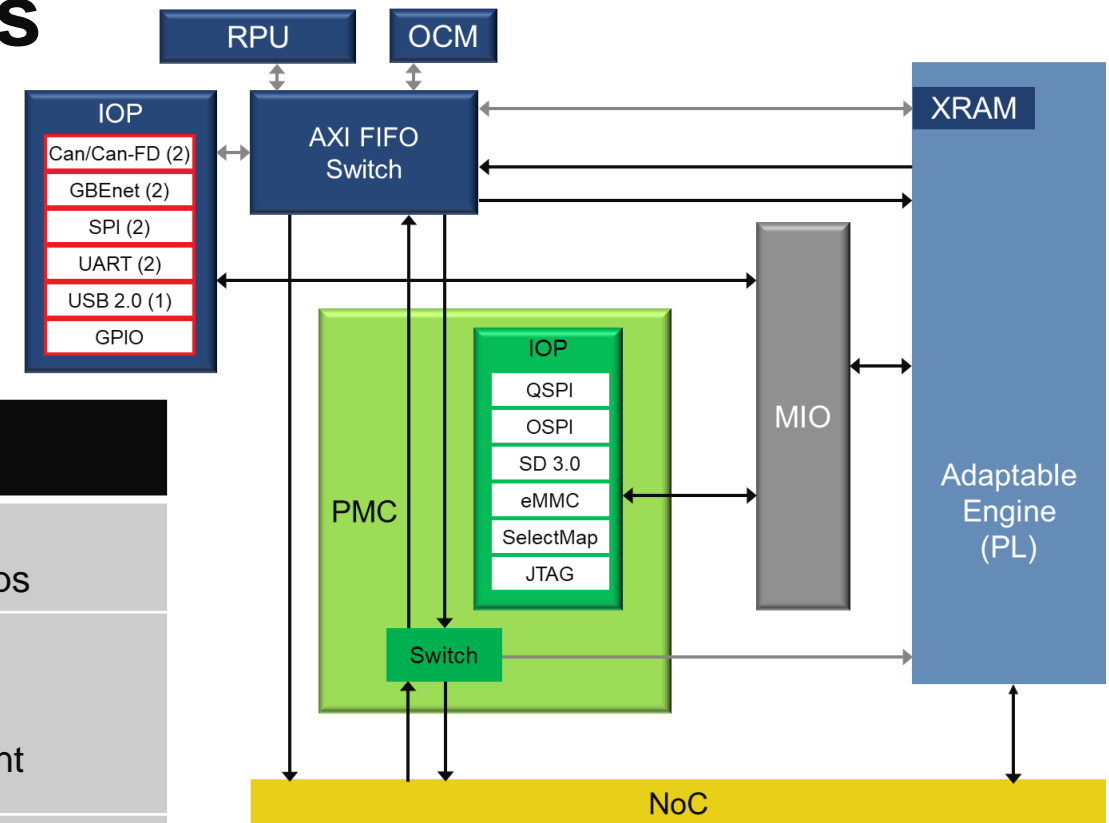


¹: DMIPS vs. Zynq UltraScale+ MPSoCs

Processing System Peripherals

- Resident in the PS

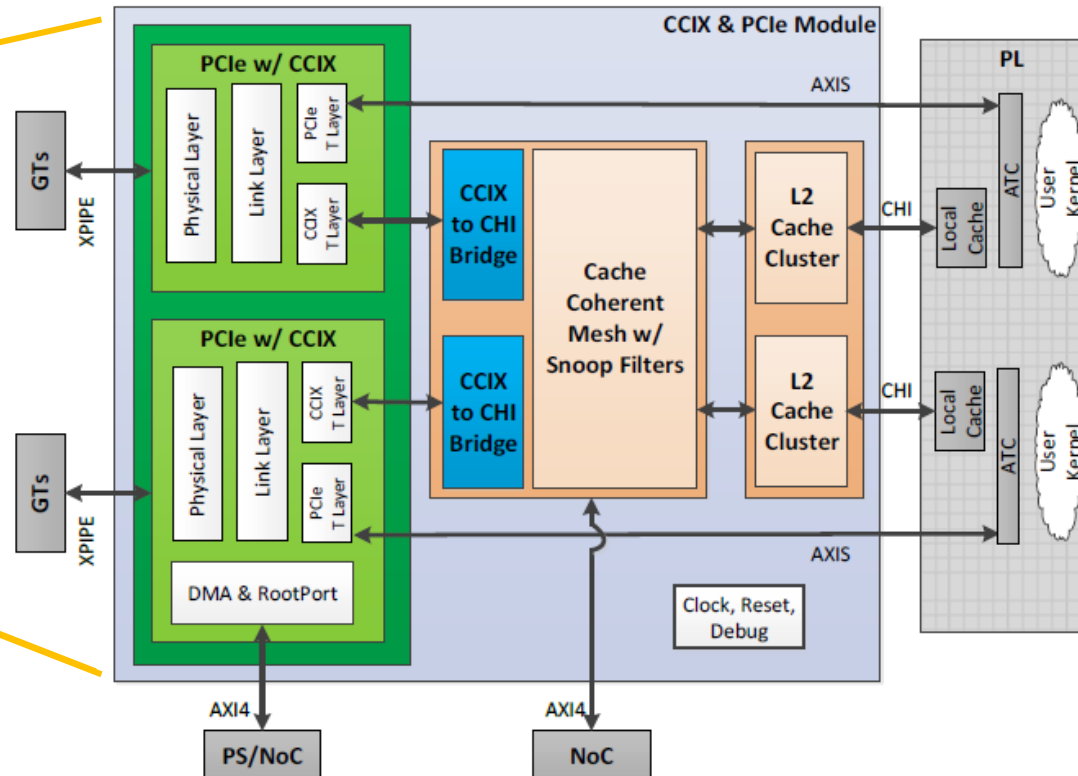
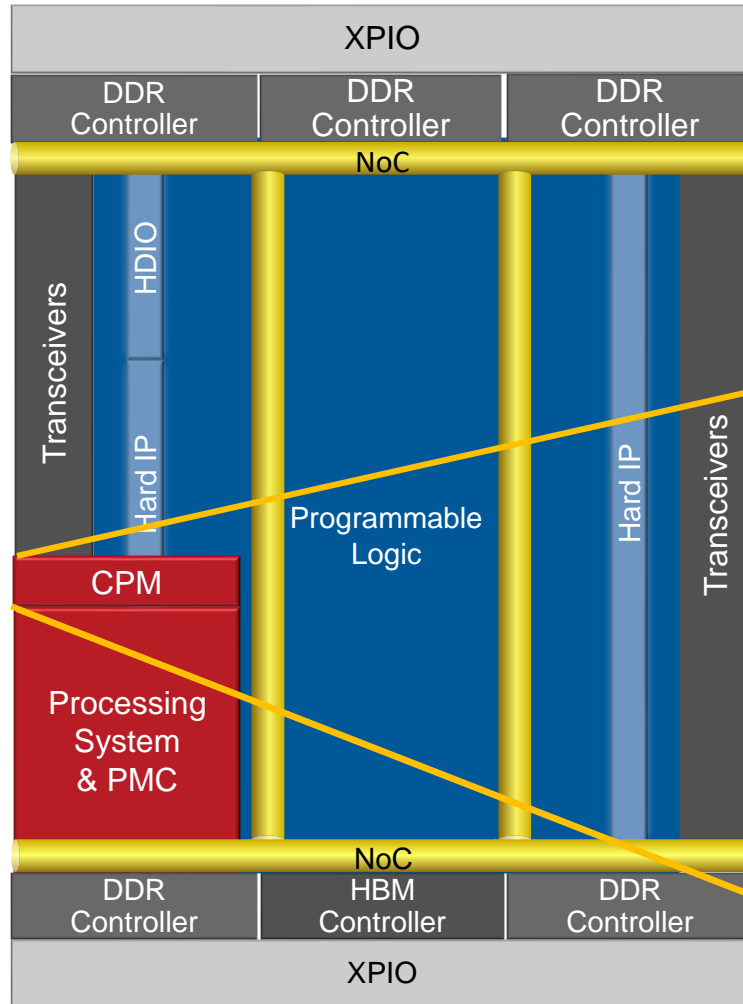
	#	PHY	Frequency (MHz)	Bandwidth (Mbit/sec)	Pinout	Notes
Gigabit Ethernet	2	SGMII	125	1250	EMIO	10/100/1000Mbps
		RGMII	125	125	MIO	
UART	2		External clock	8	MIO	SBSAv3 Level 1 Compliant
			100 (internal)	1.5		
SPI	2	Master	50		MIO	
		Slave	25		EMIO	
CAN/CAN-FD	2		Up to 80/160			1x/2x clocking required for CAN-FD
USB 2.0	1	ULPI	60	60	MIO	Device and Host, static OTG
GPIO	6 banks of 32bits (3 shareable / 3 fixed)					

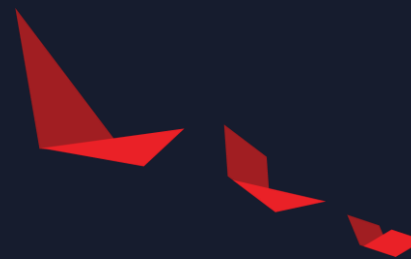


CPM Architecture View

▶ CPM - Caching & PCIe Module

- Two PCIe endpoints, one with DMA and RootPort capability
- CCIX interface layer
- AXI4MM Interconnect
- Enables coherent PCIe system without PL configuration





Boot, Configuration, and Security

New and Enhanced Versal Security Features

Zynq-7000 (28nm)

HW Root of Trust (RSA-2048)
Confidentiality (AES-CBC)
Integrity
JTAG Monitor/Disable
Test I/F Protections
Environmental Monitoring
Unique Identifiers
Run-time Config. Health
Check
TrustZone Support
Internal Key Clear (BBRAM)

Zynq UltraScale+ (16nm)

HW Root of Trust (RSA-4096)
Public Key Revocation
Confidentiality (AES-GCM)
Cryptographic Acceleration
Run-time Isolation (XPPU/XMPU)
Encrypted Key Store (PUF)
DPA Countermeasures
Software Test Libraries (STL)
FIB Resistance
In-System Key Agility (BBRAM)

Versal ACAP (7nm)

HW Root of Trust (+ECDSA)
Enhanced Key Revocation
Crypto Known Answer Tests (KAT)
AES-GCM w/Masking (DPA)
Key Index
TRNG/PRNG
Boot within Strict Env. Parameters
MACSEC (Bulk Encryption)
Glitch Detector
Tamper Logging
User Accessible PUF
Enhanced Secure Debug

Platform Management Controller (PMC)

Device Configuration

- > Boots the ACAP in milliseconds
- > PL configuration
- > 8x faster dynamic configuration
- > Octal SPI

System Monitor

- > Thermal measurements
- > Power measurements
- > Alarms

Security

- > AES-GCM encryption
- > Authentication: RSA, ECDSA
- > PUF with secure private key store
- > BBRAM
- > True random number generator

Device Integrity and Debug

- > Debug through High Speed Debug Port
- > 8x faster readback
- > Improved readback capture
- > SEU detect/correct with SEM IP

Primary Boot Devices

	Frequency – Mhz (TBD*)	SDR/DDR	Width	Max BW (Mbits/s)	IO Voltage
SD (v3.0)	50	SDR	x4	200	1.8, 3.3
	200			800	1.8
	50	DDR		400	
eMMC (v4.51)	50	SDR	x1,x4,x8	400	1.8, 3.3
	50	DDR	x4,x8	800	
	200	SDR	x4,x8	1600	1.8
Quad SPI	150	SDR	x4, 2x4, Dual Parallel	1200	1.8, 3.3
Octal SPI	200	SDR and DDR	x8, 2x8	3200	1.8
SelectMAP(slave)	200		x8,x16,x32	3200	
JTAG (slave)	100			100	

- > **Versal™ ACAP initial boot controlled by RCU**
 - >> Operates at lower frequency while the initial PLM data is read
 - >> DDR Mode not used during RCU stage
- > **Primary boot is controlled by the PLM on PPU - Scales up to higher frequency***
 - >> Bitstreams are now part of a larger data set (PDI) rather than discrete unit

* These are target frequencies, pending verification on Silicon.

Intelligent Engines

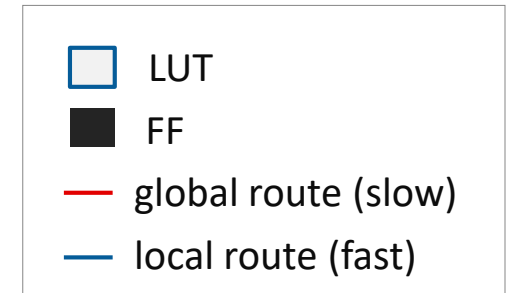
Re-Architected Logic Structure for 4X Compute Density

4X Logic Resources per CLB (vs. 16nm)

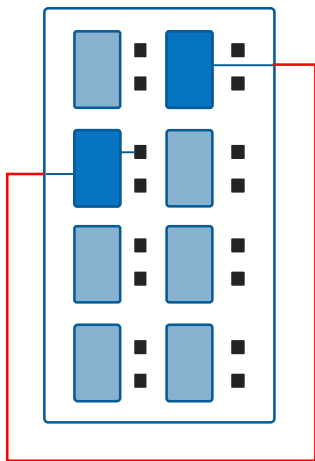
- ▶ 8 LUTs → 32 LUTs
- ▶ 16 Flip-Flops → 64 Flip-Flops

New internal CLB routing resources

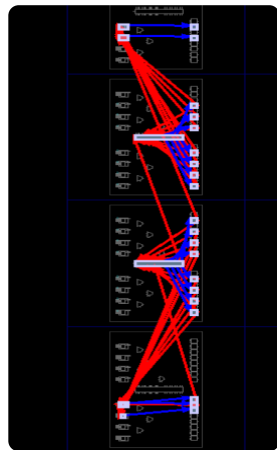
- ▶ More local routing, reduces need for global interconnect
- ▶ Increases F_{MAX} and device utilization



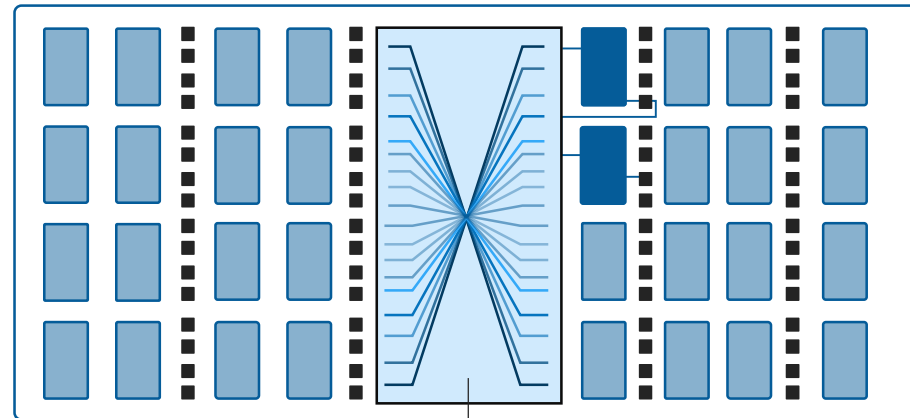
16nm UltraScale CLB



16nm 16b_counter
16 Global routes used

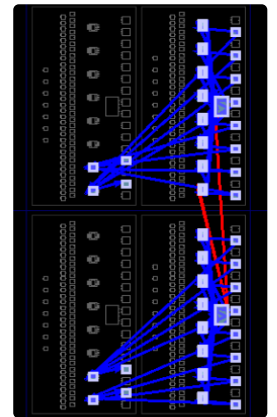


7nm Versal CLB



New CLB Interconnect

16b_counter
2 Global routes used

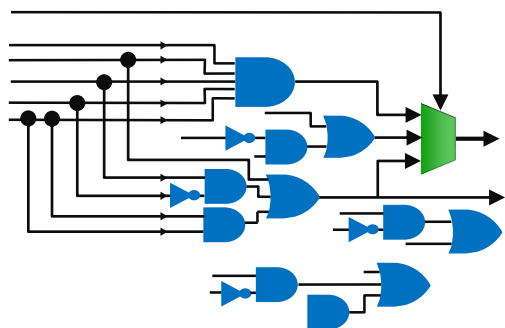


Digital Signal Processing Capability

FPGA Fabric DSP

LUT and Memory

RTL Entry



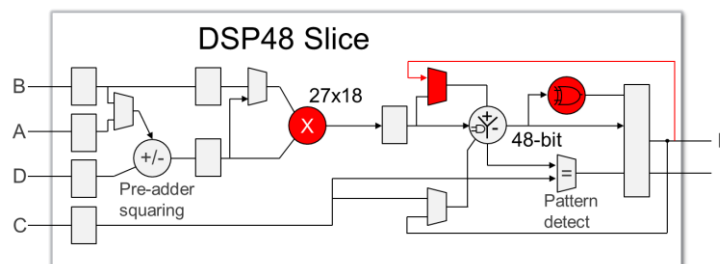
Increasing Capability

DSP48E2 Slice

Hardened MULT & ADDERS

$$ACC = ACC + (A \times B)$$

RTL Entry



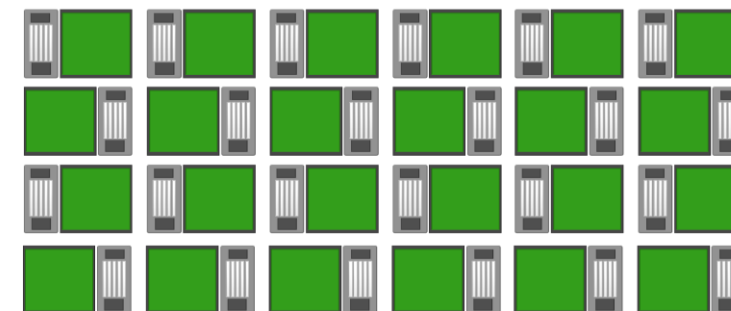
Increasing Capability

Increasing Capability

AI Engine⁽¹⁾ 2D Array

VLIW and SIMD Architecture

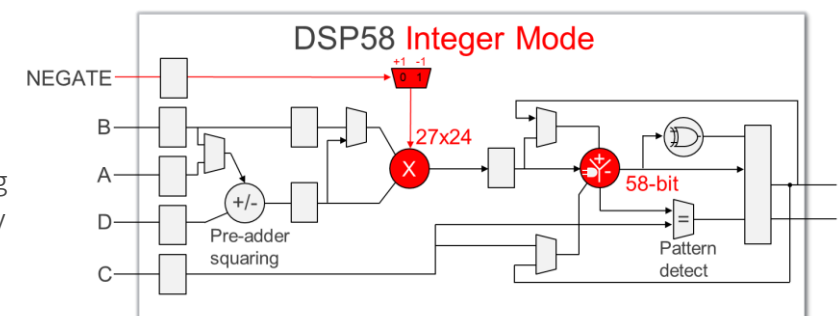
C/C++ Programmable



DSP58

Additional Features

RTL Entry



AI Engine Tile

AI Engine

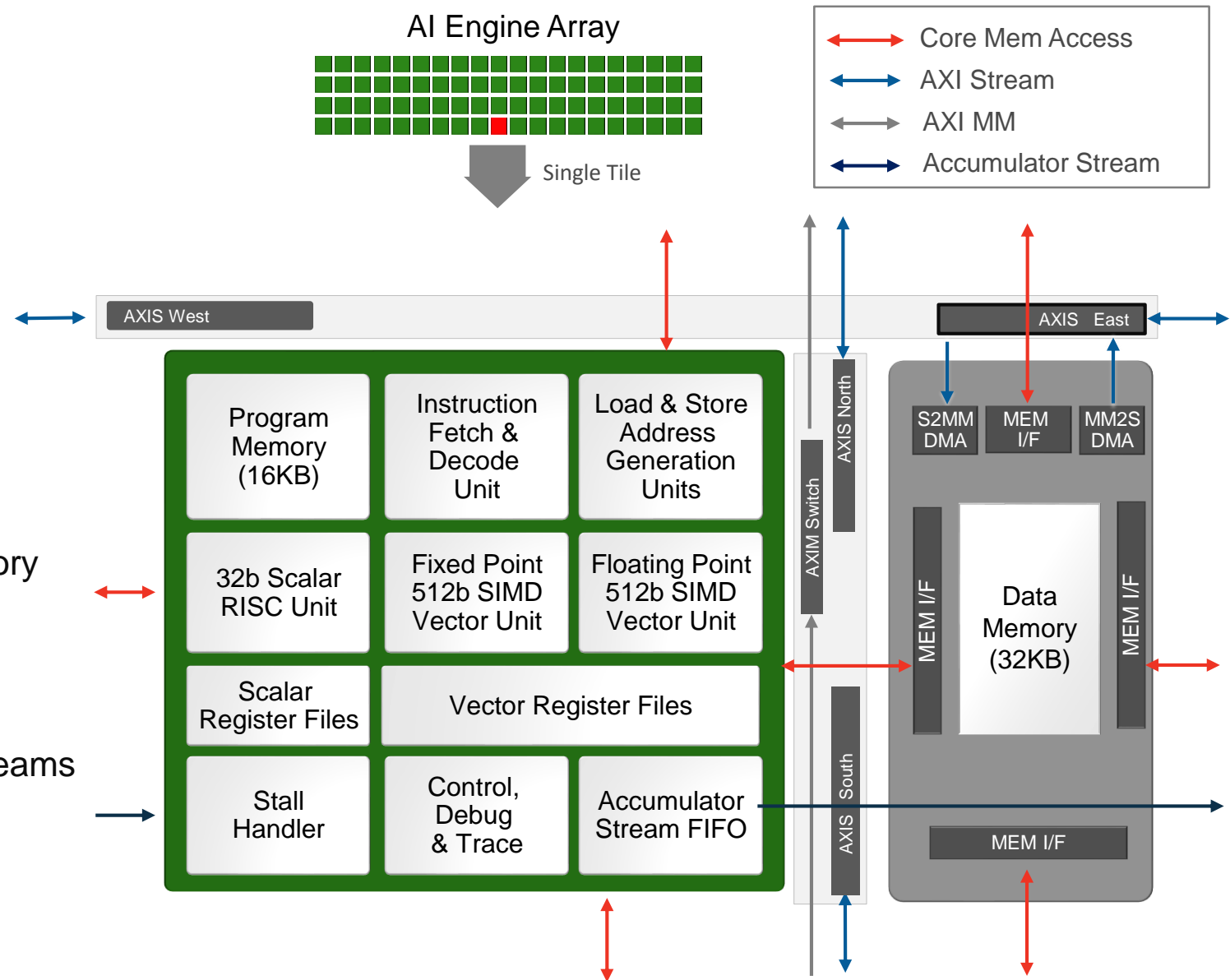
- > 1+ GHz VLIW / SIMD AI Engine
- > 32-bit Scalar RISC processor
- > Fixed and floating point vector units

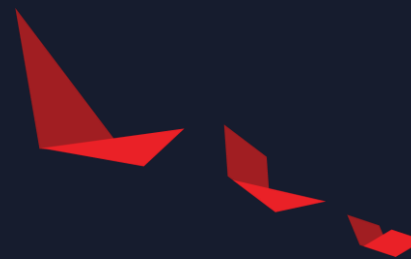
Data Memory

- > Each AI Engine can access 4 Memory Modules (N,E,S,W) as one contiguous memory

Interconnect

- > AXI-MM switch for config, control, and debug
- > AXI-Stream crossbar for routing N/E/S/W streams





Transceivers and Connectivity IP

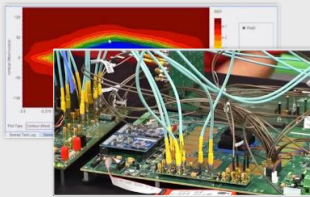
In-House SerDes Development is a *Must*

2009

28Gb/s

3rd Party

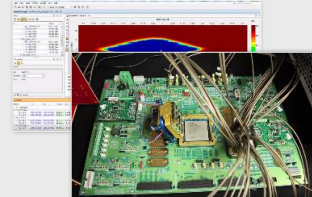
From
Test-Chip



2012

30Gb/s

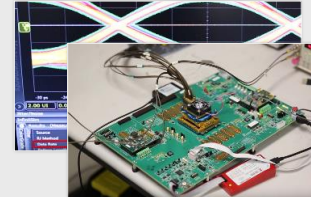
Xilinx Design



2014

33Gb/s

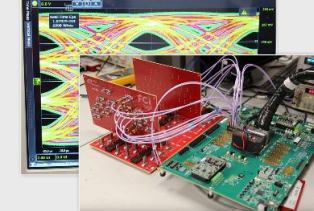
Xilinx Design



2016

58Gb/s

Xilinx Design



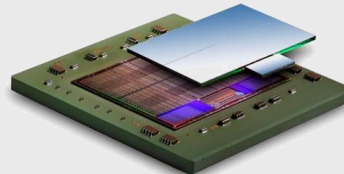
2018

112Gb/s

Xilinx Design



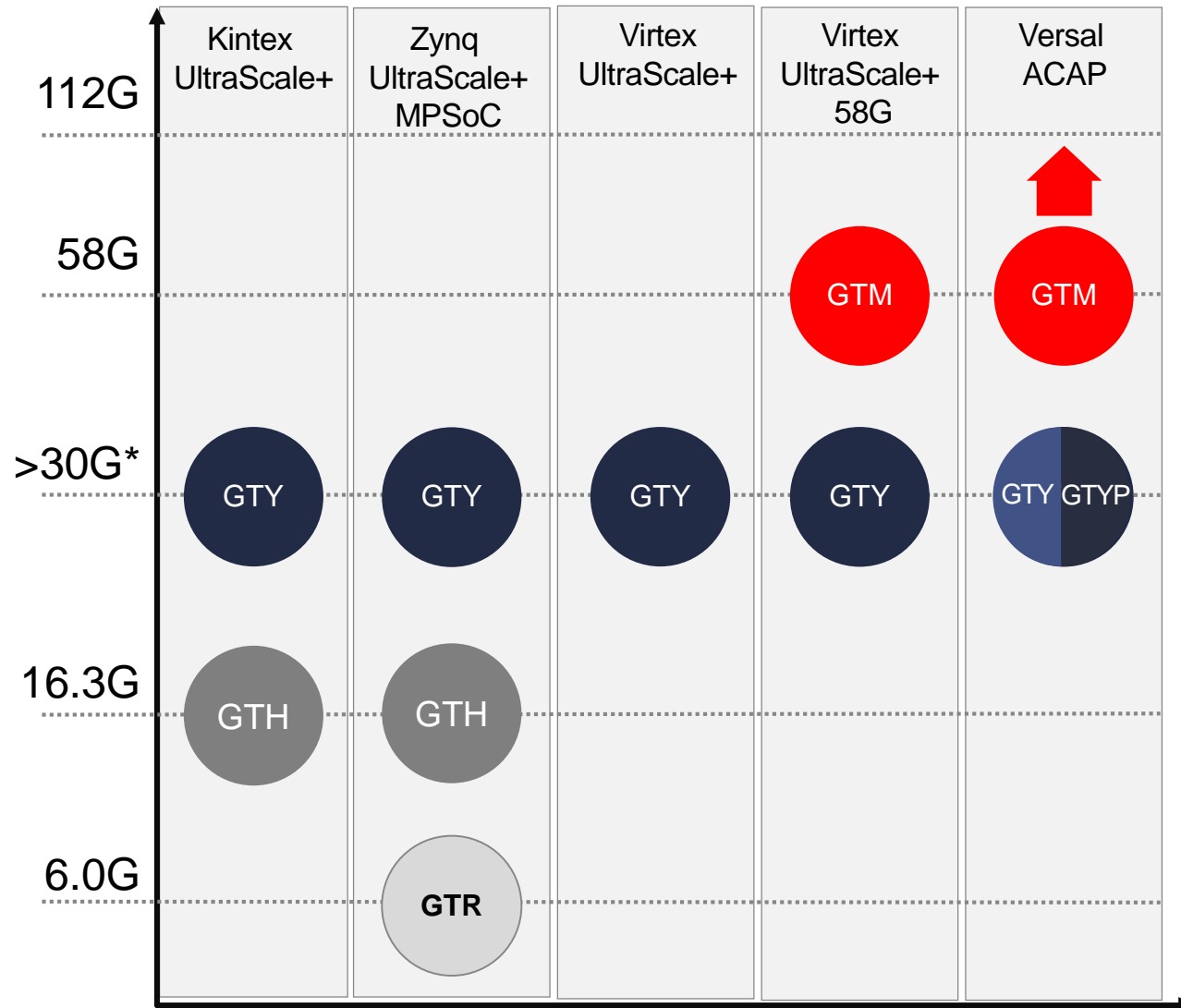
To Final
Product



Challenges with 3rd Party
SerDes Integration
(Virtex-7 HXT)



Enhanced Portfolio and More Bandwidth



*Note: 30.5G in Virtex UltraScale, 32.75G in Kintex/Virtex UltraScale+

▶ GTM Transceivers

- Tuned for the latest copper cable, backplane and optical interfaces
- Newly introduced 112G support

▶ GTY transceivers

- Optimized for latency and power reduction
- High transceiver counts to balance flexibility
- GTYP variant to support PCIe Gen5

▶ GTM & GTY in Versal ACAPs

- 112G / 58G PAM4 GTM transceivers
- 33G NRZ GTY transceivers

100G Multirate Ethernet MAC, PCS and FEC (MRMAC)

- ▶ MAC+PCS in a 4x sliced architecture, supporting the following rates:

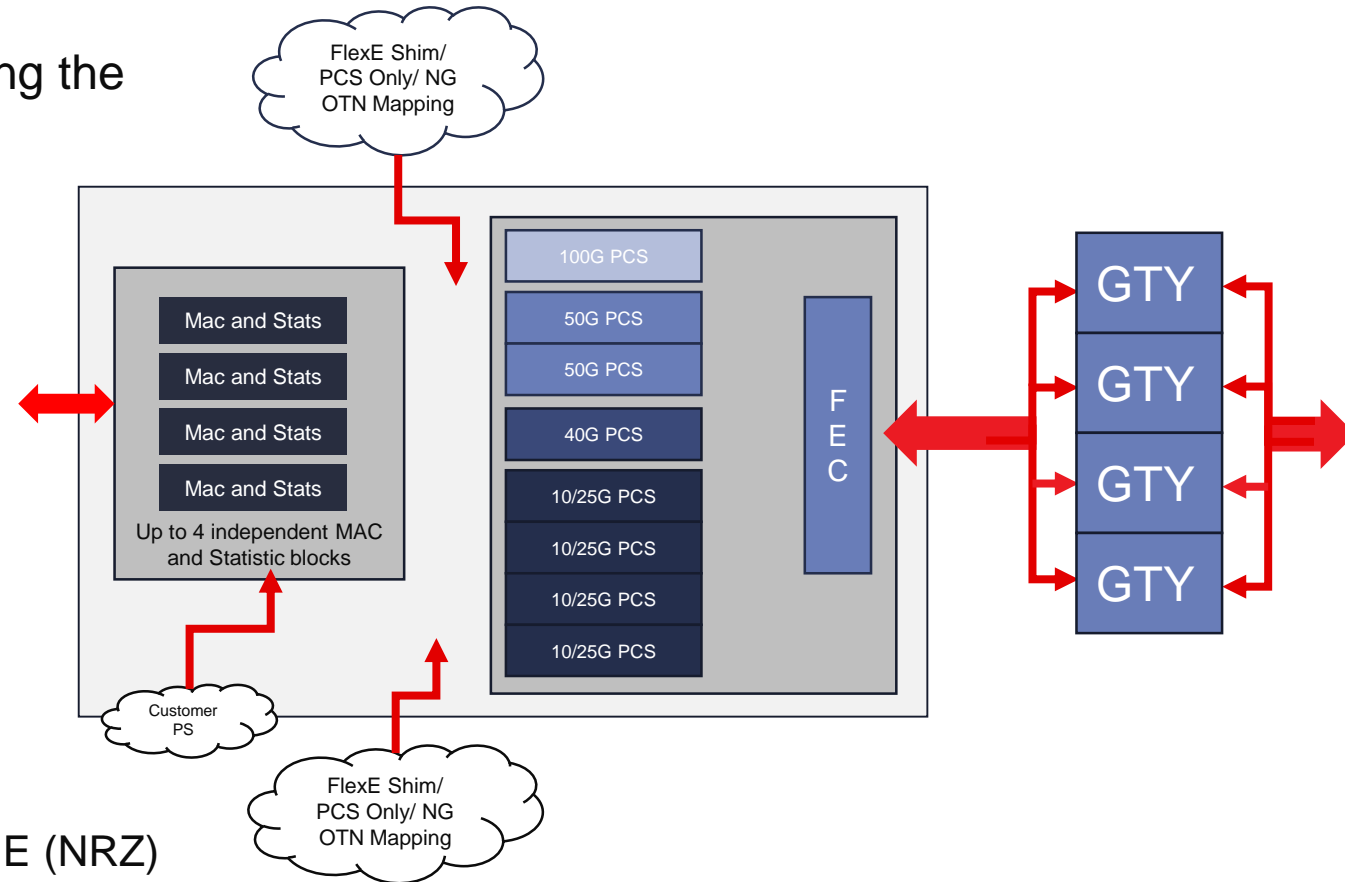
- 1x100GE
- 2x50GE
- 1x40GE
- 4x25GE
- 4x10GE

- ▶ Overclocking to support:

- 28.21Gb/s/56.42Gb/s support for 25/50/100GE
- 28.05Gb/s FC32 rate (also 24G CPRI PCS+FEC)

- ▶ Integrated FECs

- CL 91 RSFEC (528,514) KR4 FEC for 25/50/100GE (NRZ)
- CL 91 RSFEC (544,514) KP4 FEC for 50/100GE (PAM4)
- CL 74 FEC for 10/25/40/50GE (Legacy low latency FEC)



600G Ethernet MAC, PCS and FEC (DCMAC)

▶ Ethernet PCS/MAC in multiple configurations

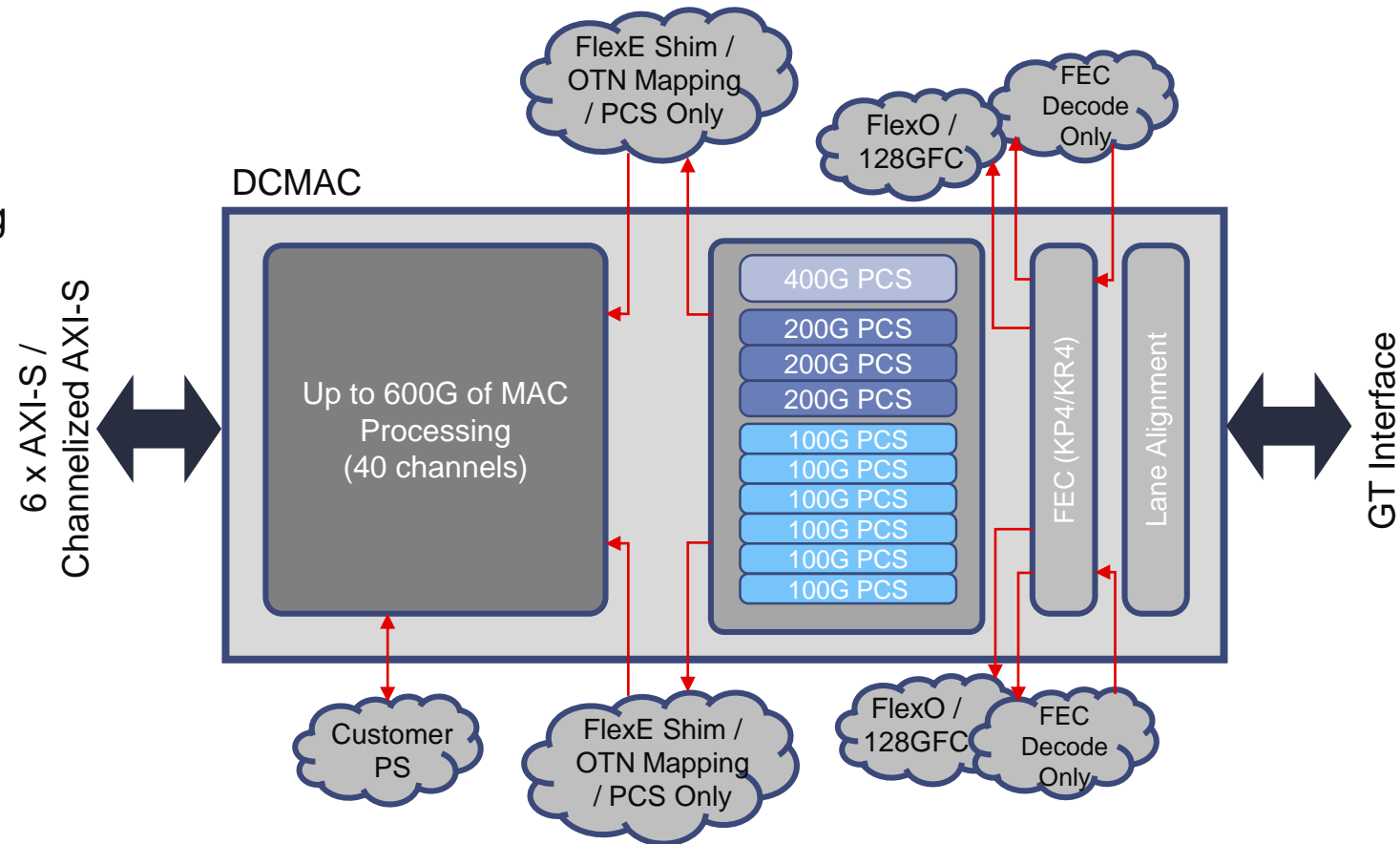
- 6 x 100G
- 3 x 200G
- 1 x 400G
- FlexE with up to 600G and 40 channels (using an fabric shim for distribution, idle and alignment control)

▶ Flexible use cases

- Sideband access for FlexE shim integration, OTN reuse, or PCS only modes
- Integrated and reusable KR4/KP4 RS-FEC
 - Use directly with MAC/PCS
 - Stand alone access for OTU or other applications

▶ Massive logic savings

- Prototypes use an entire VU9P
- Power savings in line with logic reduction



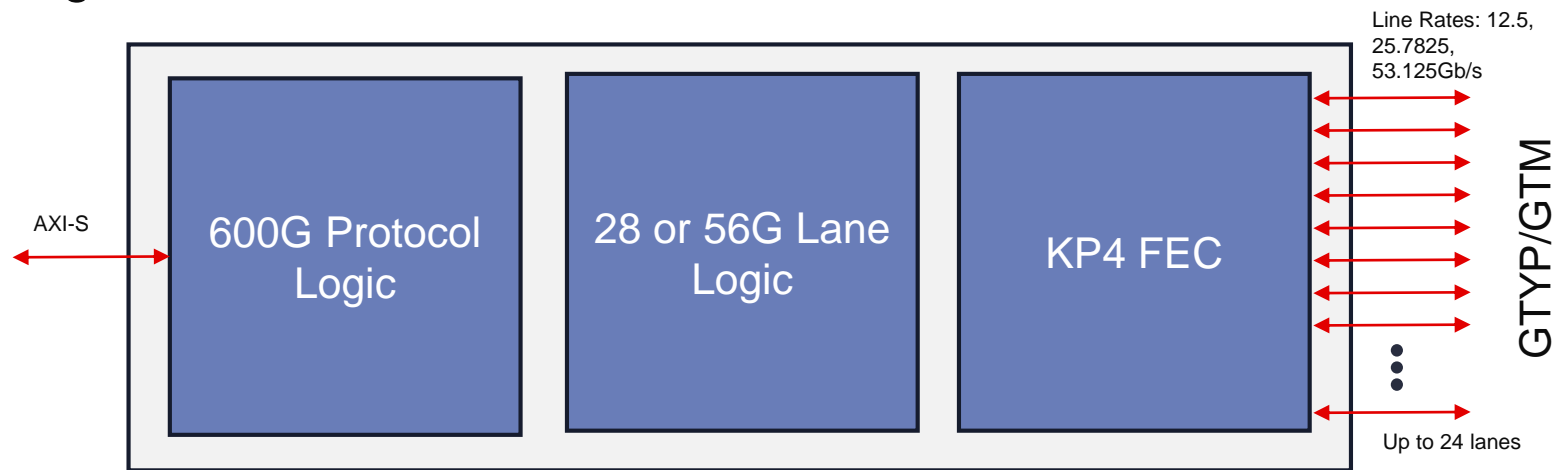
600G Interlaken

▶ Common Chip-to-chip Protocol

- Interface to FIC or other networking ASIC/ASSP
- 12.5 to 53.125Gb/s
- GTY/GTYP or GTM supported

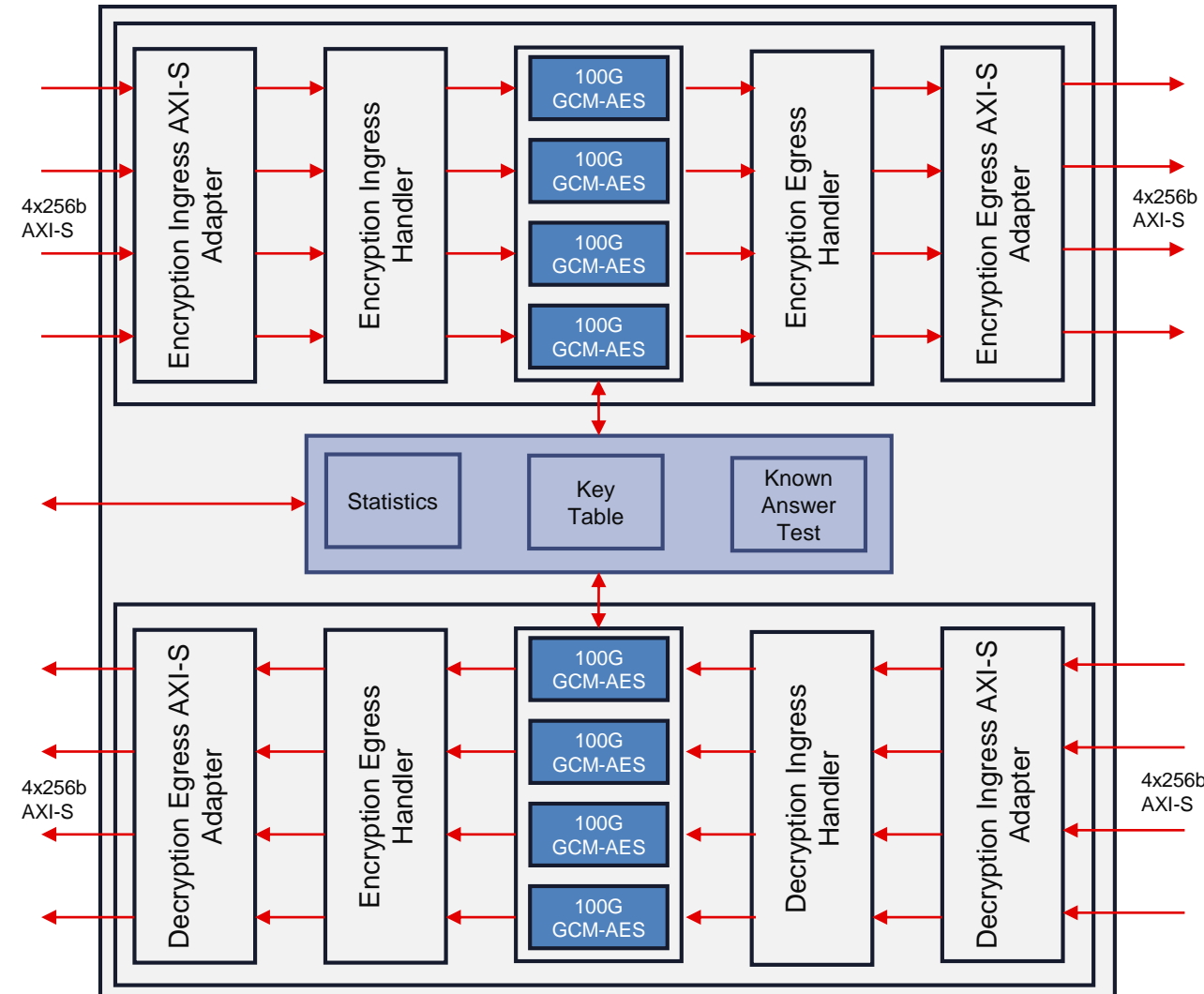
▶ Savings and Simplicity

- Integrated IP removes logic utilization requirements
- Drops power consumption drastically
- Guaranteed timing/performance



400G of Channelized Encryption

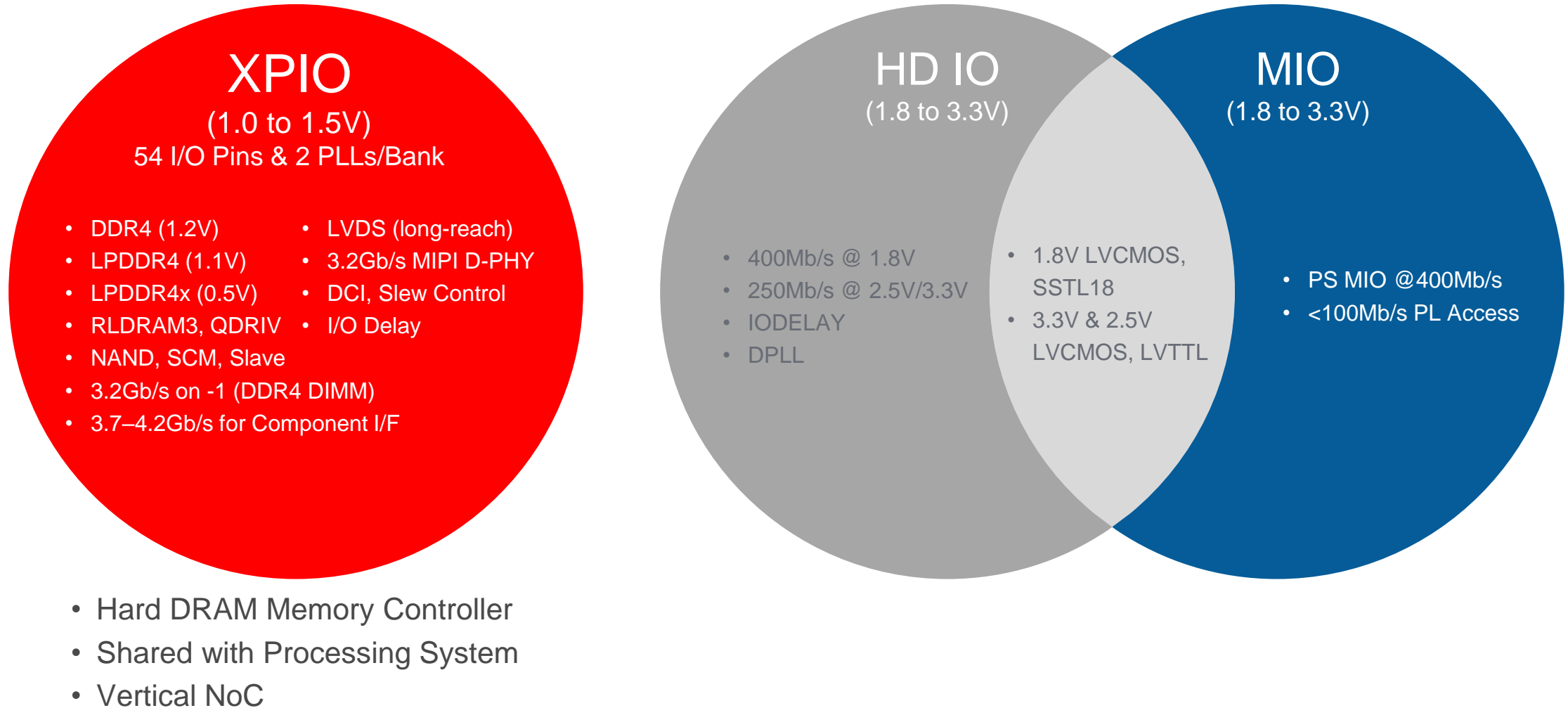
- ▶ Integrated Encrypt/Decrypt
 - Implements NIST AES-128 or -256 encryption and decryption
- ▶ MACSec
 - Securing point to point links
- ▶ IPSec
 - Securing connections over the network
- ▶ Max Bandwidth, Max Flexibility:
 - 400G of total bandwidth
 - 40 channels
 - Up to 400GE of encrypt/decrypt or
 - 40x10GE encrypt/decrypt





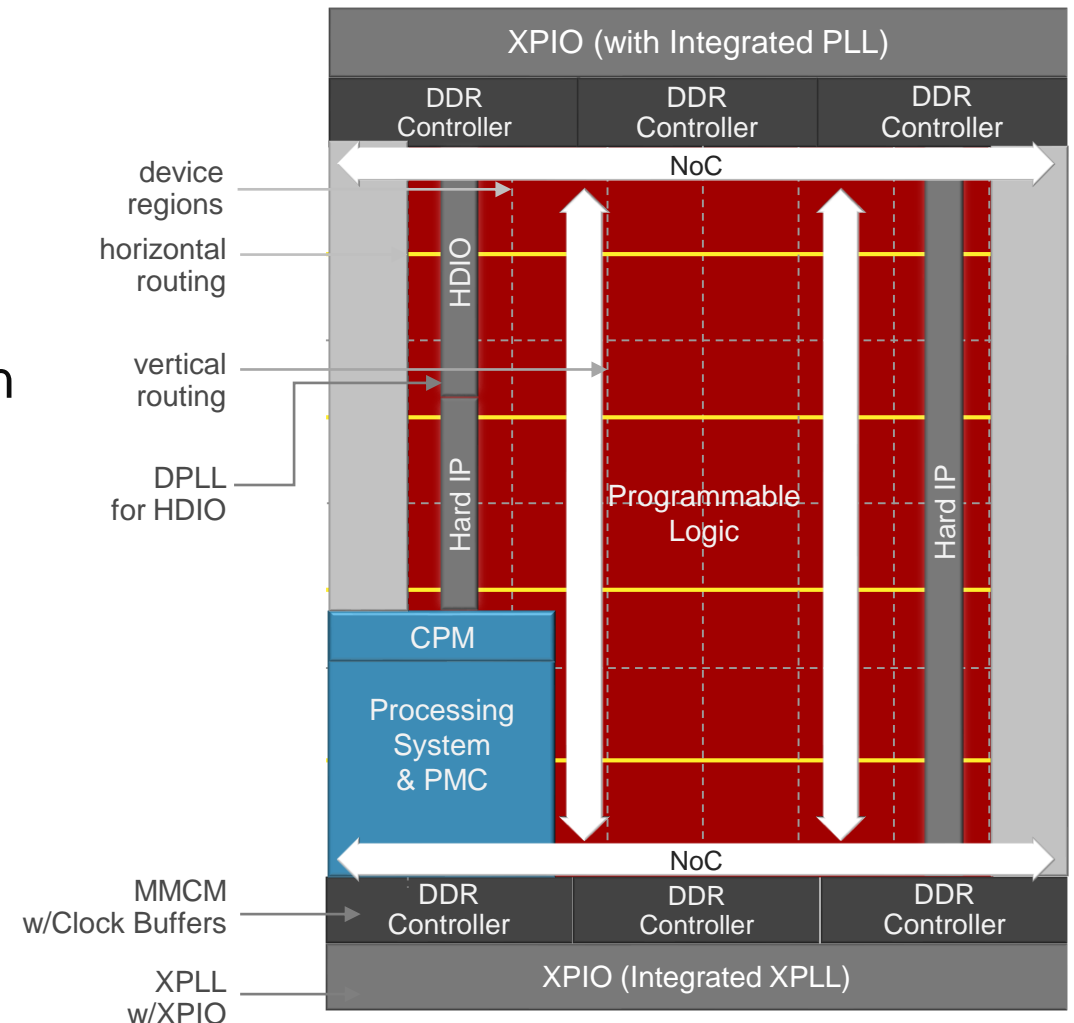
I/O, Clocking and Memory Interface

Programmable I/O



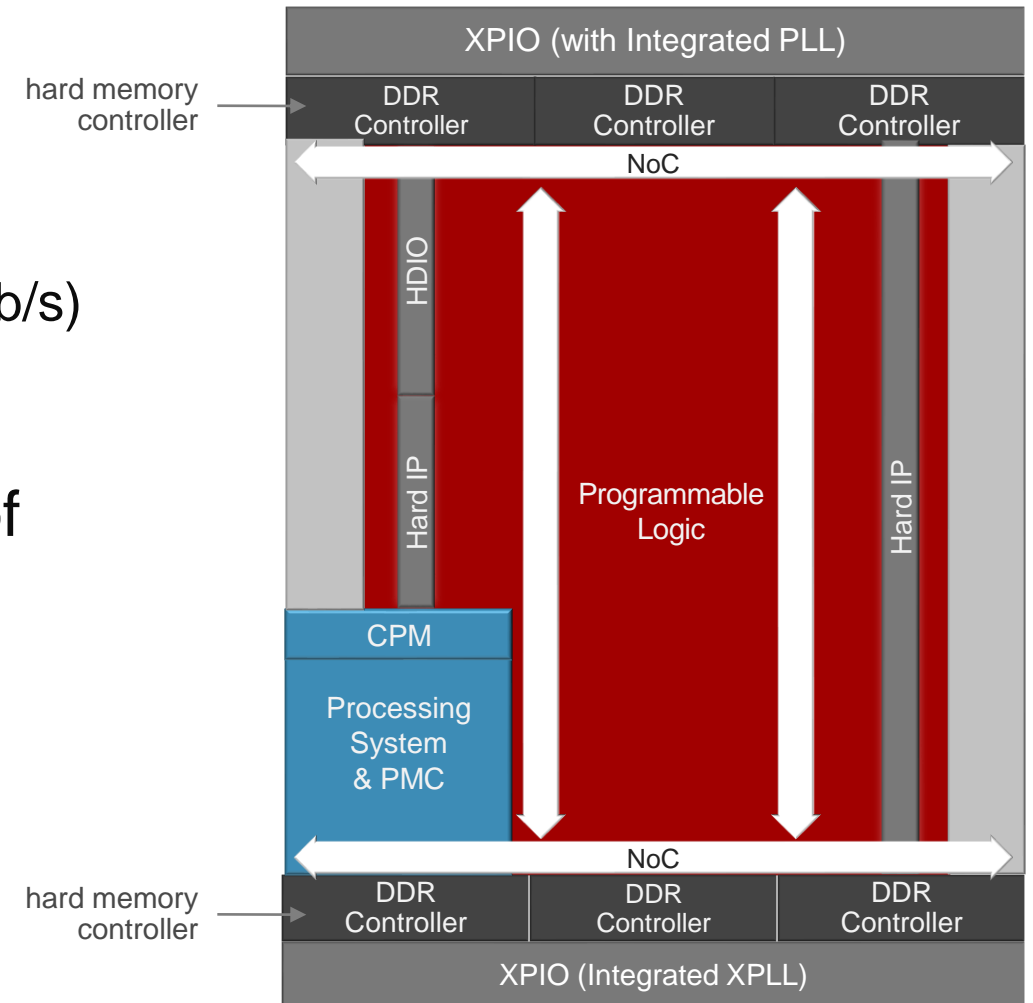
Clocking

- ▶ Global clocking network similar to UltraScale/+
 - Device broken into regions
 - Horizontal routing available in each region
 - Vertical routing adjacent to vertical NoC column
- ▶ MMCM and PLL separated
 - MMCM with clock buffers
 - XPLL with XPIO
- ▶ Additional DPLL for HDIO
 - HDIO column contains DPLL in each region
 - Also 4 BUFGs and 2 CCIO



DDR Interfaces & Hard Controller

- ▶ Dedicated hard memory controllers
 - Located at top and bottom of the device
 - Access to hard controllers via horizontal NoC
 - Support DDR4 (3200Mb/s) and LPDDR4 (4266Mb/s)
 - Optimized for x32 & x64+ECC
- ▶ Number of memory controllers a function of device size
 - Wider devices have more XPIO
- ▶ Soft PL controller with hard PHY for other configurations
 - RLDRAM3, QDRIV, DDR3L



Versal™ Prime Series

Adaptable Engines			VM1102	VM1302	VM1402	VM1502	VM1802	VM2502	VM2602	VM2902
	System Logic Cells (K)		336	605	1,119	797	1,968	1,969	1,575	2,233
	LUTs		153,472	276,480	511,488	364,544	899,840	900,224	719,872	1,020,928
Memory	Distributed RAM (Mb)		5	8	16	11	27	27	22	31
	Total Block RAM (Mb)		5	18	40	19	34	47	49	70
	Total UltraRAM (Mb)		44	50	80	60	130	190	127	181
Intelligent Engines	Total SRAM Capacity (Mb)		54	76	136	90	191	264	198	282
	DSP Engines		472	832	1,696	1,312	1,968	3,984	1,904	2,672
Scalar Engines	Application Processing Unit		Dual-core Arm® Cortex-A72, 48KB/32KB L1 Cache w/ parity & ECC; 1MB L2 Cache w/ ECC							
	Real-time Processing Unit		Dual-core Arm Cortex-R5, 32KB/32KB L1 Cache, and 256KB TCM w/ECC							
	Memory		256KB On-Chip Memory w/ECC							
	Connectivity		Ethernet (x2); USB 2.0 (x1); UART (x2); SPI (x2); I2C (x2); CAN-FD (x2)							
Foundational Platform	NoC Master / NoC Slave Ports		5	9	18	14	28	28	30	42
	DDR Bus Widths		64	128	256	128	256	256	192	192
	DDR Memory Controllers		1	2	4	2	4	4	3	3
	CCIX & PCIe® w/DMA (CPM)		-	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX	-	-
	PCI Express®		1 x Gen4x8	2 x Gen4x8	2 x Gen4x8	4 x Gen4x8	4 x Gen4x8	1 x Gen4x8	2 x Gen4x8	2 x Gen4x8
	100G Multirate Ethernet MAC		1	2	2	4	4	2	6	8
Package Footprint	Package Dimensions (mm)	Ball Pitch (mm)	XPIO, HDIO, MIO GTY, GTM	XPIO, HDIO, MIO GTY, GTM	XPIO, HDIO, MIO GTY, GTM	XPIO, HDIO, MIO GTY, GTM	XPIO, HDIO, MIO GTY, GTM	XPIO, HDIO, MIO GTY, GTM	XPIO, HDIO, MIO GTY, GTM	XPIO, HDIO, MIO GTY, GTM
B625	21x21	0.8	216, 22, 78 4, 0							
B1024	31x31	0.92	216, 22, 78 12, 0	216, 22, 78 16, 0	324, 22, 78 16, 0					
B1369	35x35	0.92		216, 22, 78 24, 0	324, 22, 78 24, 0	378, 22, 78 16, 0				
F1369	35x35	0.92		324, 22, 78 8, 0	648, 22, 78 8, 0					
A1760	40x40	0.92		432, 22, 78 24, 0	648, 22, 78 24, 0				486, 22, 78 8, 24	
C1760	40x40	0.92				378, 44, 78 44, 0	378, 44, 78 44, 0		378, 44, 78 8, 40	378, 44, 78 8, 40
D1760	40x40	0.92					648, 0, 78 24, 0			
A2197	45x45	0.92					648, 44, 78 44, 0	648, 22, 78 16, 16		

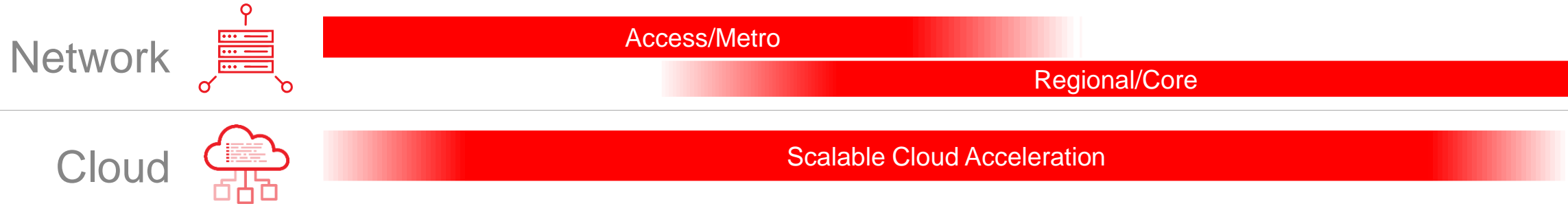
Notes:

1. GTY transceivers operate at data rates up to 32.75Gb/s.
2. GTM transceivers operate at data rates up to 58Gb/s.

Versal™ AI Core Series

		VC1352	VC1502	VC1702	VC1802	VC1902
Intelligent Engines	AI Engines	128	248	320	300	400
	AI Engine Data Memory Blocks (#)	1024	1984	2560	2400	3200
	AI Engine Data Memory (Mb)	32	62	80	75	100
Adaptable Engines	DSP Engines	928	1,312	1,696	1,600	1,968
	System Logic Cells (K)	540	797	1,051	1,586	1,968
	LUTs	246,784	364,544	480,256	725,000	899,840
Memory	Distributed RAM (Mb)	8	11	15	22	27
	Total Block RAM (Mb)	16	19	29	28	34
	UltraRAM (Mb)	59	60	113	91	130
	Accelerator RAM (Mb)	32	0	32	0	0
	Total SRAM Capacity (Mb)	115	90	189	141	191
Scalar Engines	Application Processing Unit	Dual-core Arm® Cortex-A72, 48KB/32KB L1 Cache w/ parity & ECC; 1MB L2 Cache w/ ECC				
	Real-time Processing Unit	Dual-core Arm Cortex-R5, 32KB/32KB L1 Cache, and 256KB TCM w/ECC				
	Memory	256KB On-Chip Memory w/ECC				
	Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)				
Foundational Platform	NoC Master / NoC Slave Ports	10	14	18	28	28
	DDR Bus Width	128	128	128	256	256
	DDR Memory Controllers	2	2	2	4	4
	CCIX & PCIe® w/DMA (CPM)	–	1 x Gen4x16, CCIX	–	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX
	PCI Express®	1 x Gen4x8	4 x Gen4x8	1 x Gen4x8	4 x Gen4x8	4 x Gen4x8
	100G Multirate Ethernet MAC	1	4	3	4	4
	SD-FEC	2	0	5	0	0
	Platform Management Controller	Boot, Security, Safety, Monitoring, and High Speed Debug				
Package Footprint	Package Dimensions (mm)	Ball Pitch (mm)	XPIO, HDIO, MIO, GTY	XPIO, HDIO, MIO, GTY	XPIO, HDIO, MIO, GTY	XPIO, HDIO, MIO, GTY
A1024	31x31	0.92	378, 22, 78, 8	378, 22, 78, 8		
E1369	35x35	0.92	378, 44, 78, 8		378, 44, 78, 24	
G1369	35x35	0.92		378, 44, 78, 24		
A1596	37.5x37.5 ⁽²⁾	0.92		378, 44, 78, 32	378, 44, 78, 32	378, 44, 78, 32
D1760	40x40	0.92			648, 0, 78, 24	648, 0, 78, 24
A2197	45x45	0.92		378, 44, 78, 44	648, 44, 78, 44	648, 44, 78, 44

Versal™ Premium Portfolio: Scalable for Network & Cloud



		VP1102	VP1202	VP1402	VP1502	VP1552	VP1702	VP1802
Engines	System Logic Cells	1.6M	2.0M	2.2M	3.8M	3.8M	5.6M	7.4M
	Adaptable Engines (LUTs)	720K	900K	1M	1.7M	1.8M	2.5M	3.4M
	Intelligent Engines (DSP Slices)	1.9K	4K	2.7K	7.4K	7.4K	11K	14K
	Scalar Engines	Dual-Core Arm® Cortex®-A72 Application Processing Unit / Dual-Core Arm Cortex-R5F Real-Time Processing Unit						
IP Cores	PCIe® Gen5x8 w/DMA & CCIX	-	2	-	2	2	2	2
	PCIe Gen5x4 w/CXL ¹	2	2	2	2	8	2	2
	100G Multirate Ethernet MAC	6	2	6	4	4	6	8
	600G Ethernet MAC	4	1	8	3	1	5	7
	600G Interlaken	2	0	2	1	0	2	3
	400G High-Speed Crypto Engines	3	1	5	2	2	3	4

1: CXL implemented via a combination of hard and soft IP

Silicon Rollout

Versal Prime Series–Initial Device Availability

Schedule is tentative and subject to change

Versal Prime Series		ES1 ^(2, 3) ES9780		Production ^(2, 3)	
Device ^(1, 4)	Pkg ⁽²⁾	OOE	Avail	OOE	Avail
VM1802	A2197, D1760, C1760	NOW	NOW	Feb'21	Apr'21
VM1402	D1760, C1596, F1369, B1369, B1024	Production-Only Tapeout		H1'22	H1'22
VM1302	D1760, C1596, F1369, B1369, B1024	Production-Only Tapeout		H1'22	H1'22
VM2502	C2197	H2'21	H2'21	H2'22	H2'22
VM1502	C1760, B1369	Production-Only Tapeout		H1'22 (H2'22)	H2'22
VM2902	F1760	Production-Only Tapeout		H1'23	H1'23
VM2302	F1760	Production-Only Tapeout		H1'23	H1'23
VM1102	A784	H2'22	H2'22	H2'23	H2'23

Silicon Rollout cont'd

Versal AI Core Series—Initial Device Availability

Schedule is tentative and subject to change

Versal AI Core Series		ES1 ^(2, 3) ES9780		Production ^(2, 3)	
Device ^(1, 4)	Pkg ⁽²⁾	OOE	Avail	OOE	Avail
VC1902	A2197, D1760, A1596	NOW	NOW	Feb'21	Mar'21
VC1802	A2197, D1760, A1596	Production-Only Tapeout		Feb'21	Apr'21
VC1502	A2197, A1596, G1369, A1024	Production-Only Tapeout		H1'22	H2'22
VC1702	A1596, E1369	H1'23	H1'23	H1'24	H2'24
VC1352	E1369	Production-Only Tapeout		H2'24	H2'24

Notes

1. 'Available' means part is released for shipment. For specific delivery commits use the [Pre-order Entry Tool](#) & lead times at the time of placement of order.
2. Packages listed in order of availability. OOE and Availability dates are for the first package.
3. Dates specified should be assumed to be the end of the half/quarter/month. Dates shown are for -1 and -2 speed grade, E, and I temperature grades, as applicable.
4. Contact the PLM for Pre-ES or Pre-Production silicon availability, or with any additional feedback/questions regarding dates.

Silicon Rollout cont'd

Versal Premium Series–Initial Device Availability

Schedule is tentative and subject to change

Versal Premium Series		ES1 ^(2, 3) ES9780		Production ^(2, 3)	
Device ^(1, 4)	Pkg ⁽²⁾	OOE	Avail	OOE	Avail
VP1202	A2785, C2197	Q3'21	Q3'21	H2'22	H2'22
VP1802	C4072	Q4'21	Q4'21	H2'22	H2'22
VP1502	A2785, A3340	Q4'21 (Q3'21)	Q4'21	H2'22	H2'22
VP1702	A3340, C4072	Q4'21	Q1'22	H2'22	H2'22
VP1402	A3340, A2785, F1760	Production Only Tapeout		H1'23	H1'23
VP1102	A2785, F1760	Production Only Tapeout		H1'23	H1'23
VP1552	A2785, A3340	Production Only Tapeout		H1'23	H1'23

Notes

1. 'Available' means part is released for shipment. For specific delivery commits use the [Pre-order Entry Tool](#) & lead times at the time of placement of order.
2. Packages listed in order of availability. OOE and Availability dates are for the first package.
3. Dates specified should be assumed to be the end of the half/quarter/month. Dates shown are for -1 and -2 speed grade, E, and I temperature grades, as applicable.
4. Contact the PLM for Pre-ES or Pre-Production silicon availability, or with any additional feedback/questions regarding dates.

Summary

- ▶ ACAP is a new class of device from Xilinx
- ▶ Versal ACAPs contain some revolutionary new features
 - High-bandwidth network-on-chip
 - Breakthrough acceleration and compute capability with dedicated AI Engine
 - Latest Versal Premium series adds a vast amount of networking IP
- ▶ Go to www.xilinx.com/versal to learn more



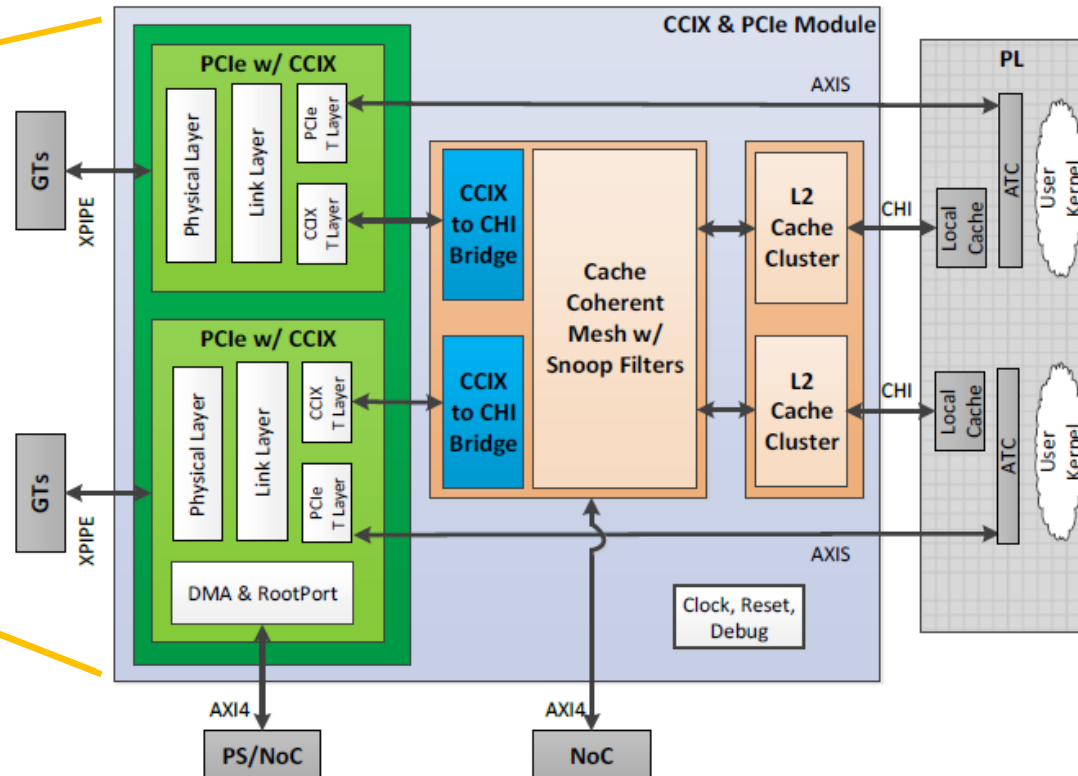
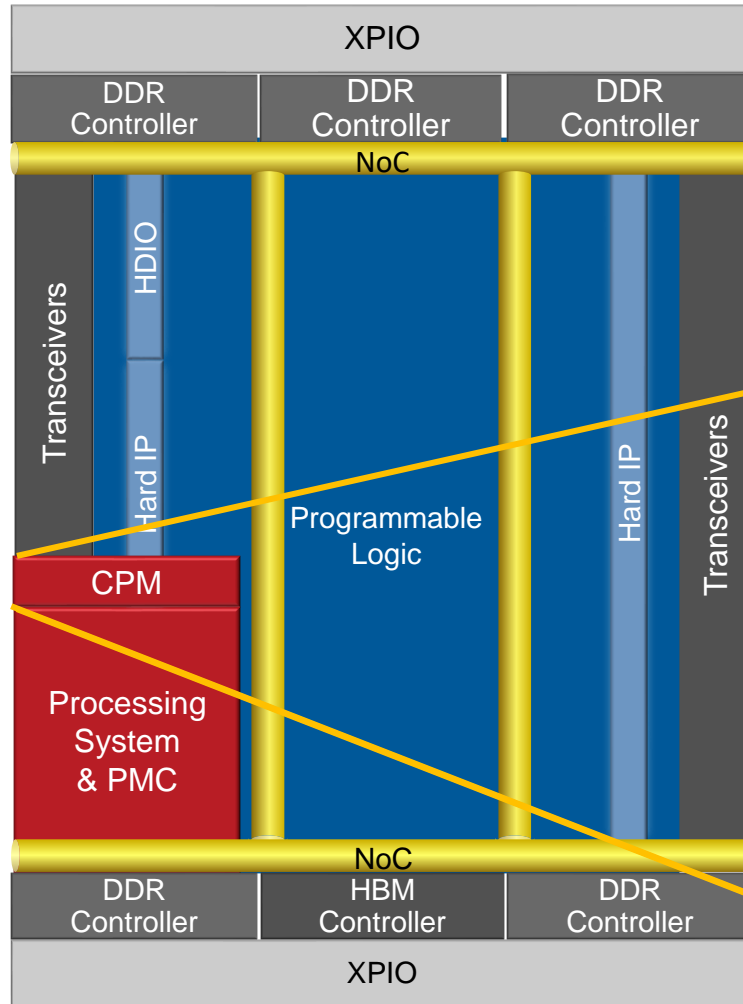
Thank You



CPM Architecture View

▶ CPM - Caching & PCIe Module

- Two PCIe endpoints, one with DMA and RootPort capability
- CCIX interface layer
- AXI4MM Interconnect
- Enables coherent PCIe system without PL configuration



New and Enhanced Versal Security Features

Zynq-7000 (28nm)

HW Root of Trust (RSA-2048)
Confidentiality (AES-CBC)
Integrity
JTAG Monitor/Disable
Test I/F Protections
Environmental Monitoring
Unique Identifiers
Run-time Config. Health
Check
TrustZone Support
Internal Key Clear (BBRAM)

Zynq UltraScale+ (16nm)

HW Root of Trust (RSA-4096)
Public Key Revocation
Confidentiality (AES-GCM)
Cryptographic Acceleration
Run-time Isolation (XPPU/XMPU)
Encrypted Key Store (PUF)
DPA Countermeasures
Software Test Libraries (STL)
FIB Resistance
In-System Key Agility (BBRAM)

Versal ACAP (7nm)

HW Root of Trust (+ECDSA)
Enhanced Key Revocation
Crypto Known Answer Tests (KAT)
AES-GCM w/Masking (DPA)
Key Index
TRNG/PRNG
Boot within Strict Env. Parameters
MACSEC (Bulk Encryption)
Glitch Detector
Tamper Logging
User Accessible PUF
Enhanced Secure Debug

Adaptable Engines

Adaptable Memory Hierarchy

▶ Distributed memory

- 50% of LUTs

▶ Block RAM

- 36Kb per block
- Dual port
- Two independent clocks

▶ UltraRAM

- 288Kb
- Dual port
- Single clock

	Block RAM	UltraRAM
Block size	36Kb	288Kb
# blocks	Up to 5,153	Up to 2,673
Total	181Mb	752Mb
Port width	X9, x18, x36, x72	X9, x18, x36, x72
Port width	Mixed on ports A and B	Mixed on ports A and B
Reset	Sync or async	Sync or async
Cascade	Within region	Full column
Fmax	1000MHz	738MHz
O/P register	INIT/SRVAL	Reset to 0
FIFO	Not supported	Not supported
ECC	1 Enc, 1 Dec per block	1 Enc, 1 Dec per port
Initialization	Any value	Any value
Power saving	Sleep and shutdown	Sleep and shutdown

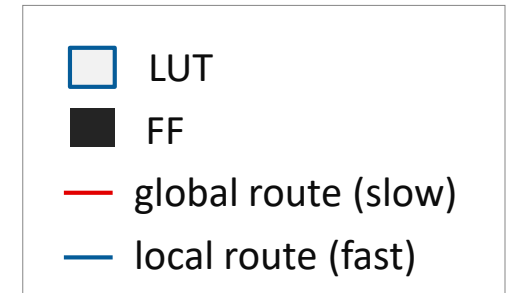
Re-Architected Logic Structure for 4X Compute Density

4X Logic Resources per CLB (vs. 16nm)

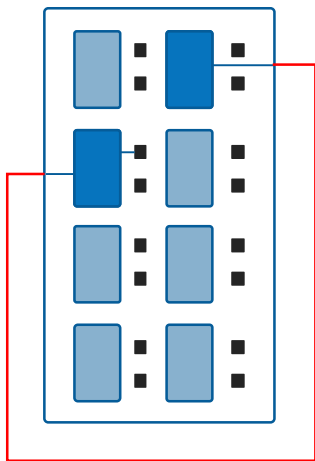
- ▶ 8 LUTs → 32 LUTs
- ▶ 16 Flip-Flops → 64 Flip-Flops

New internal CLB routing resources

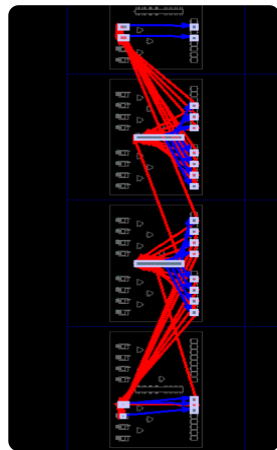
- ▶ More local routing, reduces need for global interconnect
- ▶ Increases F_{MAX} and device utilization



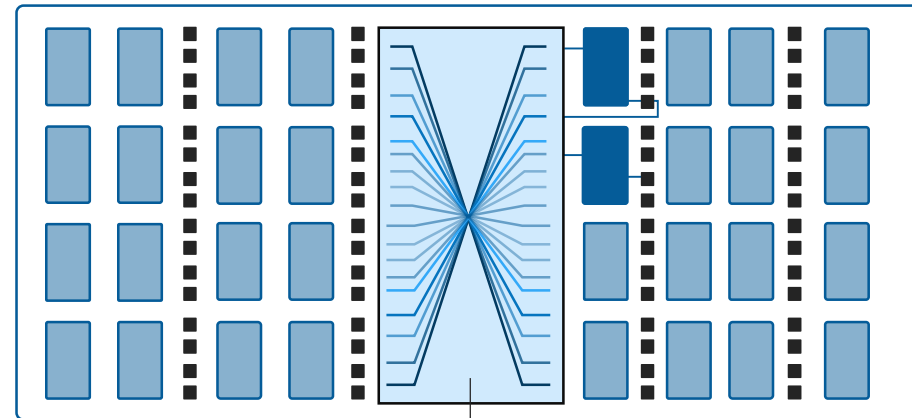
16nm UltraScale CLB



16nm 16b_counter
16 Global routes used



7nm Versal CLB



New CLB Interconnect

16b_counter
2 Global routes used

